

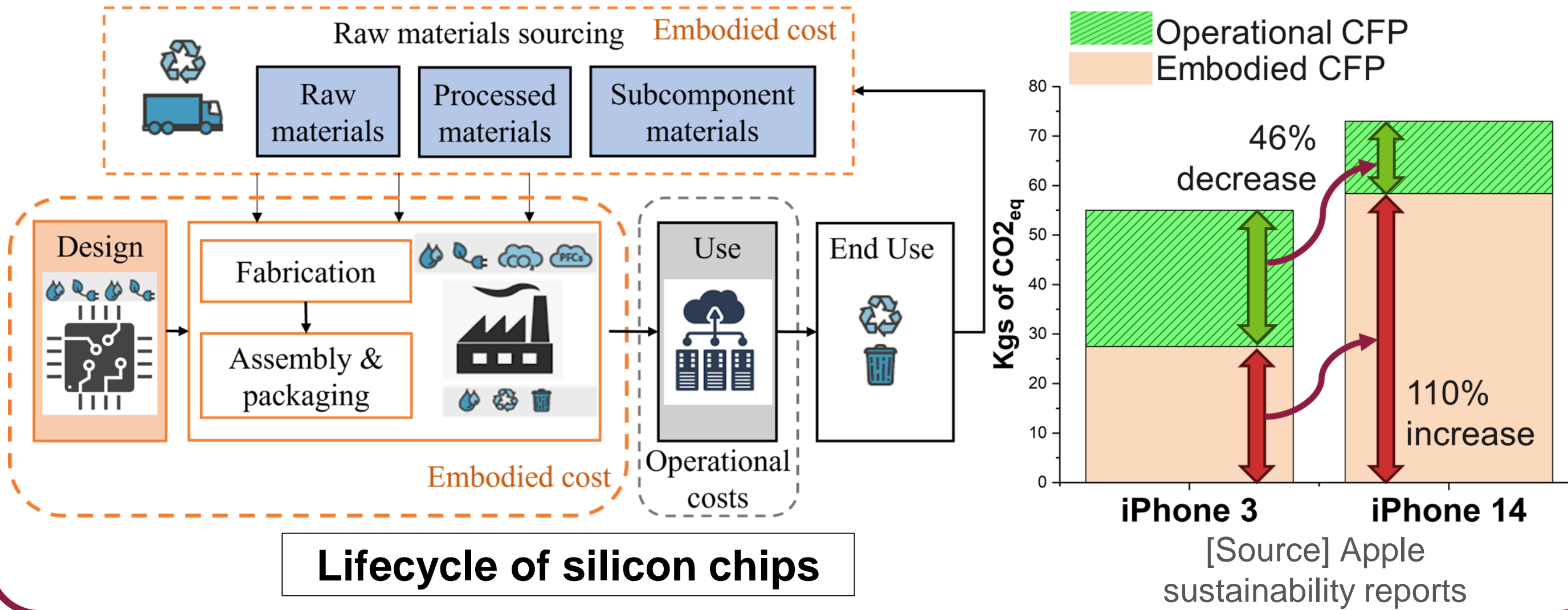
ECO-CHIP: Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI

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Introduction and background

- The information and computing **technology (ICT) industry** **contributes to 3-5%** of the world's total carbon footprint (CFP)
- The industry has focused on optimizing power, performance, and area of chips but **has neglected environmental impacts**
- Embodied CFP has increased over time due to:
 - Lower yields in newer technology nodes
 - Increased time required for design closure



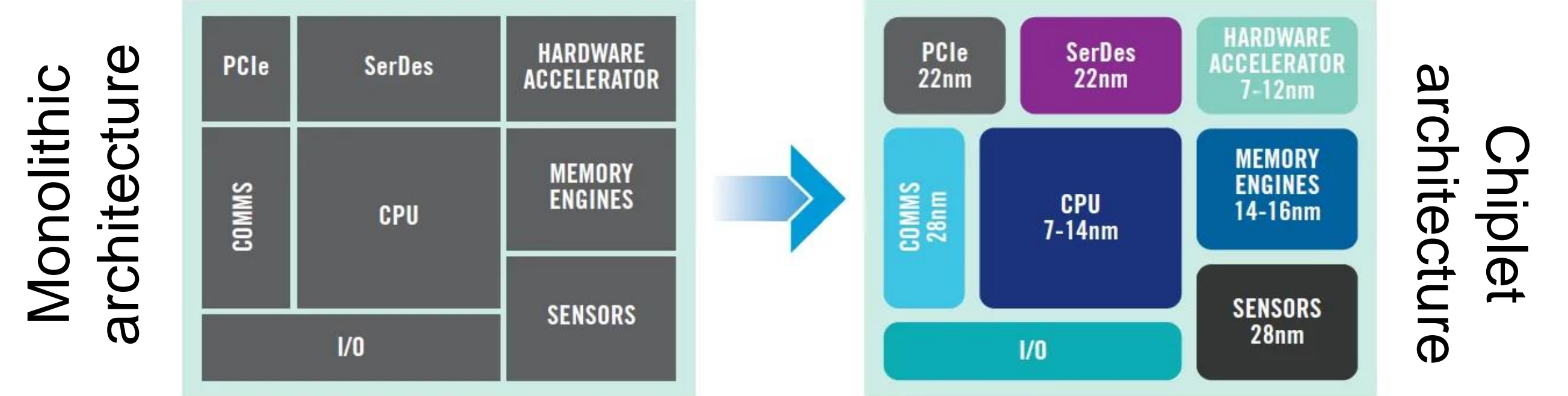
Prior work and our contributions

ACT: Architectural carbon modeling tool [Gupta et. al. ISCA 2022]

- Modeled embodied carbon
- Assumed constant packaging overheads

Our key contributions:

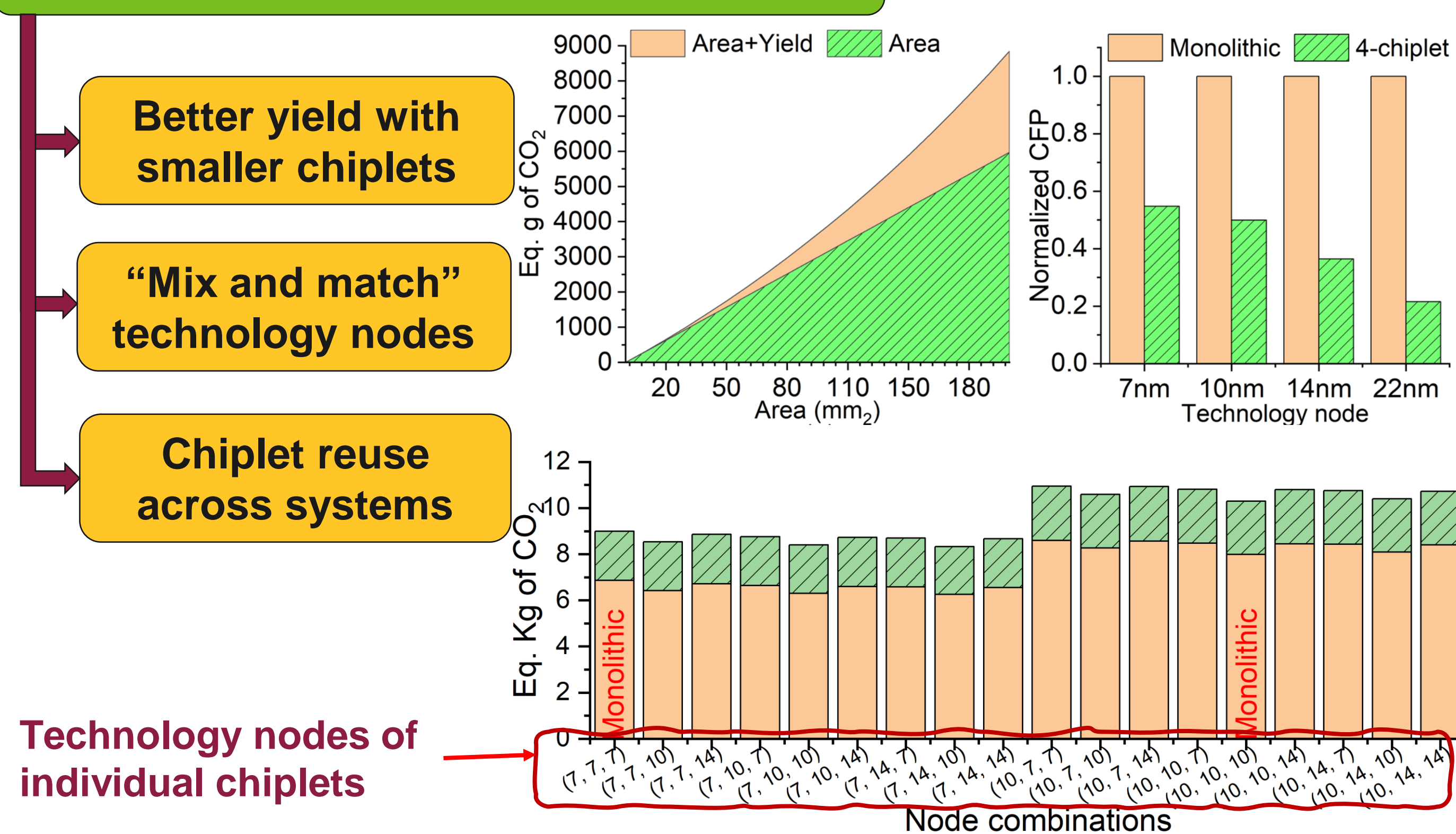
- Proposed **heterogenous integration (HI)** for sustainability
- Developed a **tool for CFP analysis for heterogeneous systems**
- Developed CFP models for **advanced packaging technologies**
- Developed CFP models for design



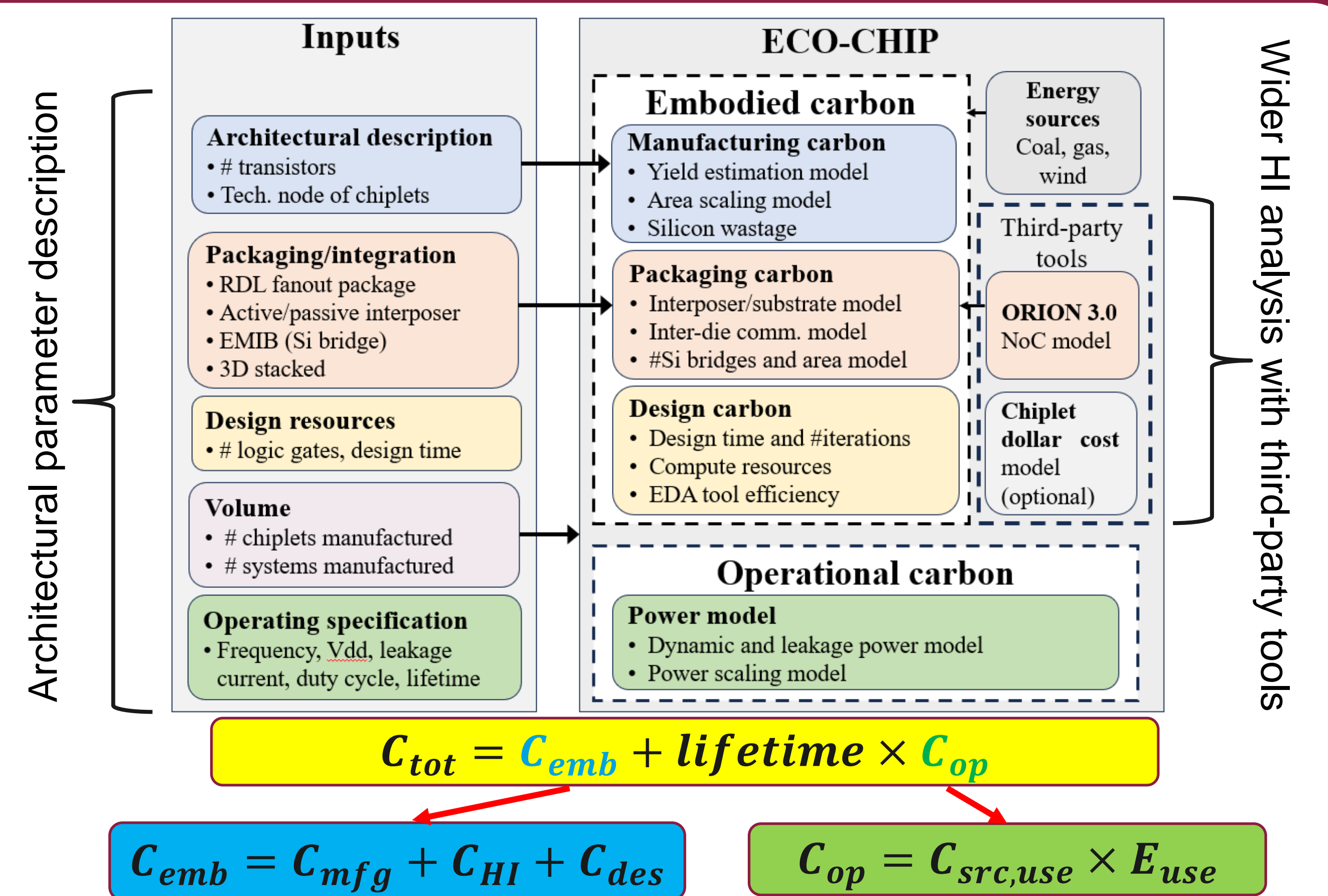
What is HI? Multiple chiplets manufactured individually and integrated into a single advanced package to sustain Moore's law

HI as a path towards sustainability

Sustainable computing via HI



ECO-CHIP framework: Total CFP model



ECO-CHIP: Embodied CFP models

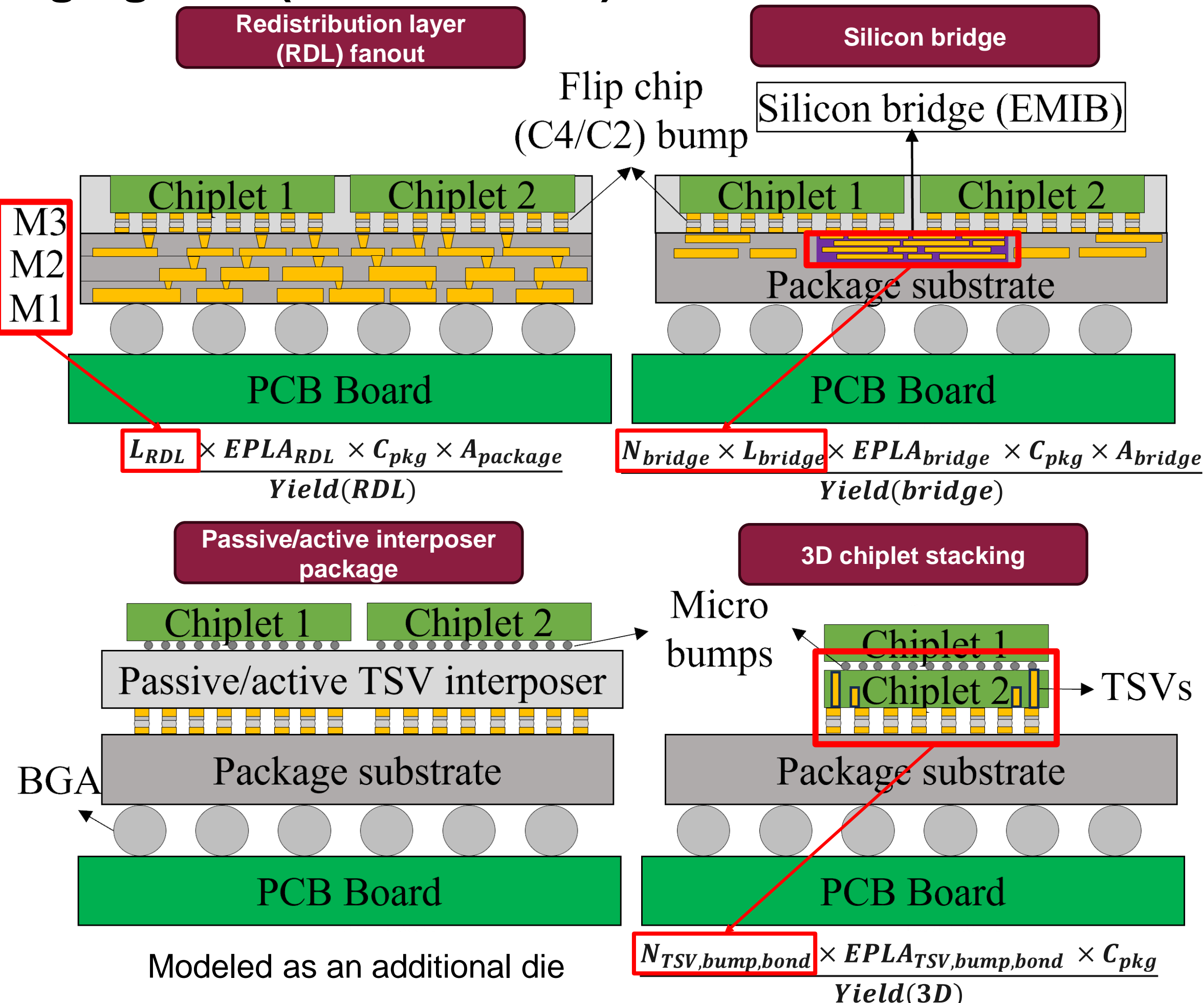
Manufacturing CFP:

$$C_{mfg} = CFPA (Die\ area + Wasted\ area)$$

Design CFP:

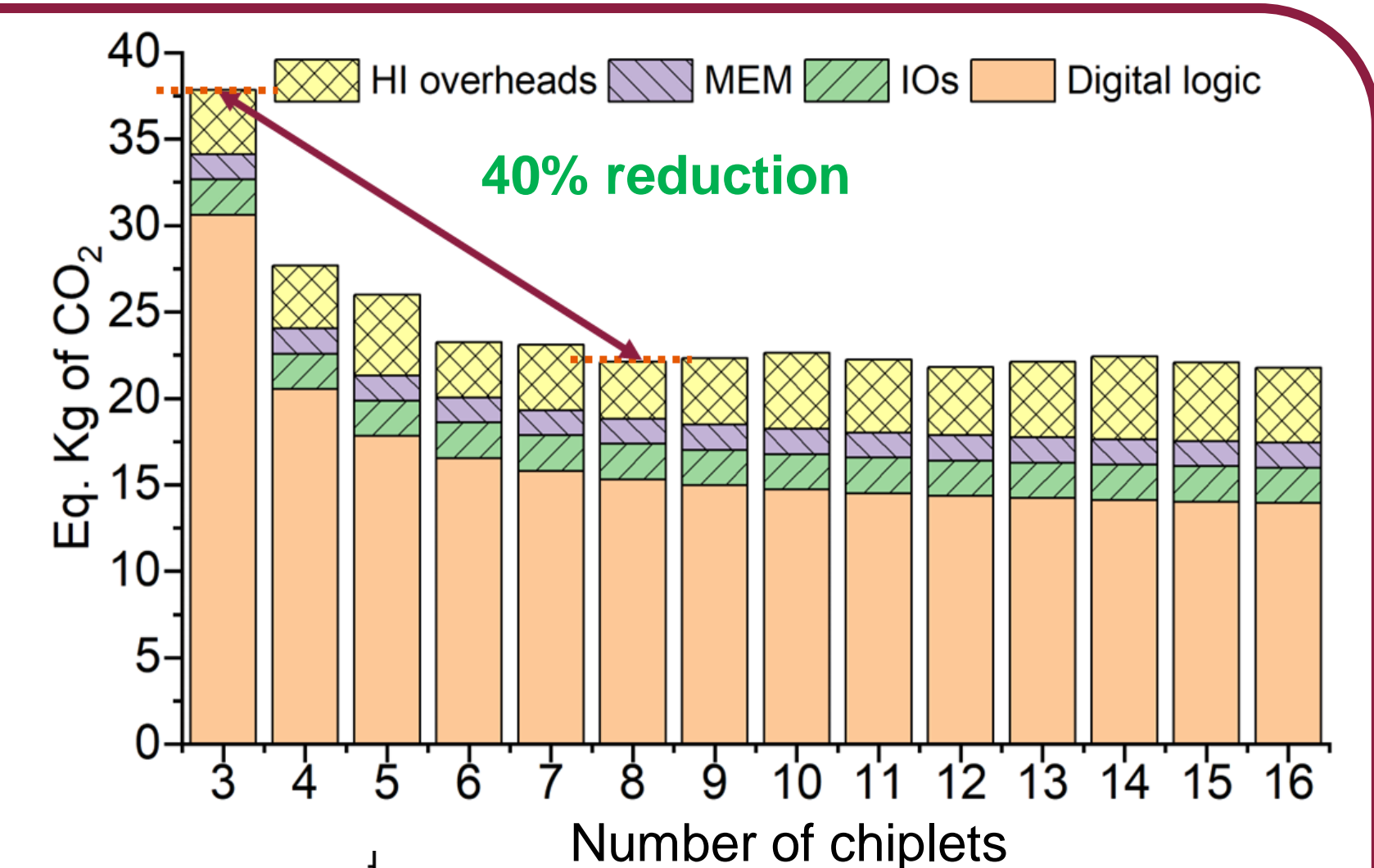
$$C_{des} = t_{des} \times P_{des} \times C_{src}$$
$$t_{des} = \frac{t_{verif} + (t_{SP\&R} + t_{analyze}) \times N_{des}}{\eta_{EDA}}$$

Packaging CFP (HI overheads):

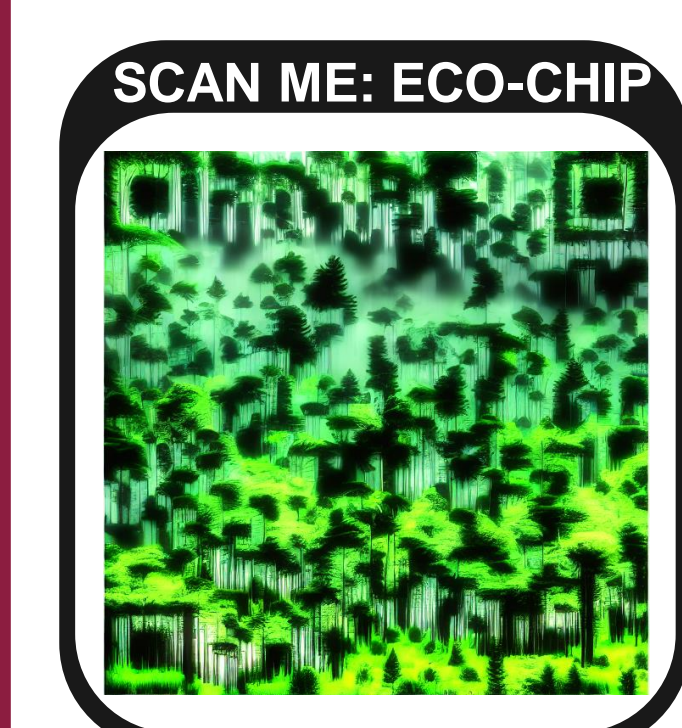
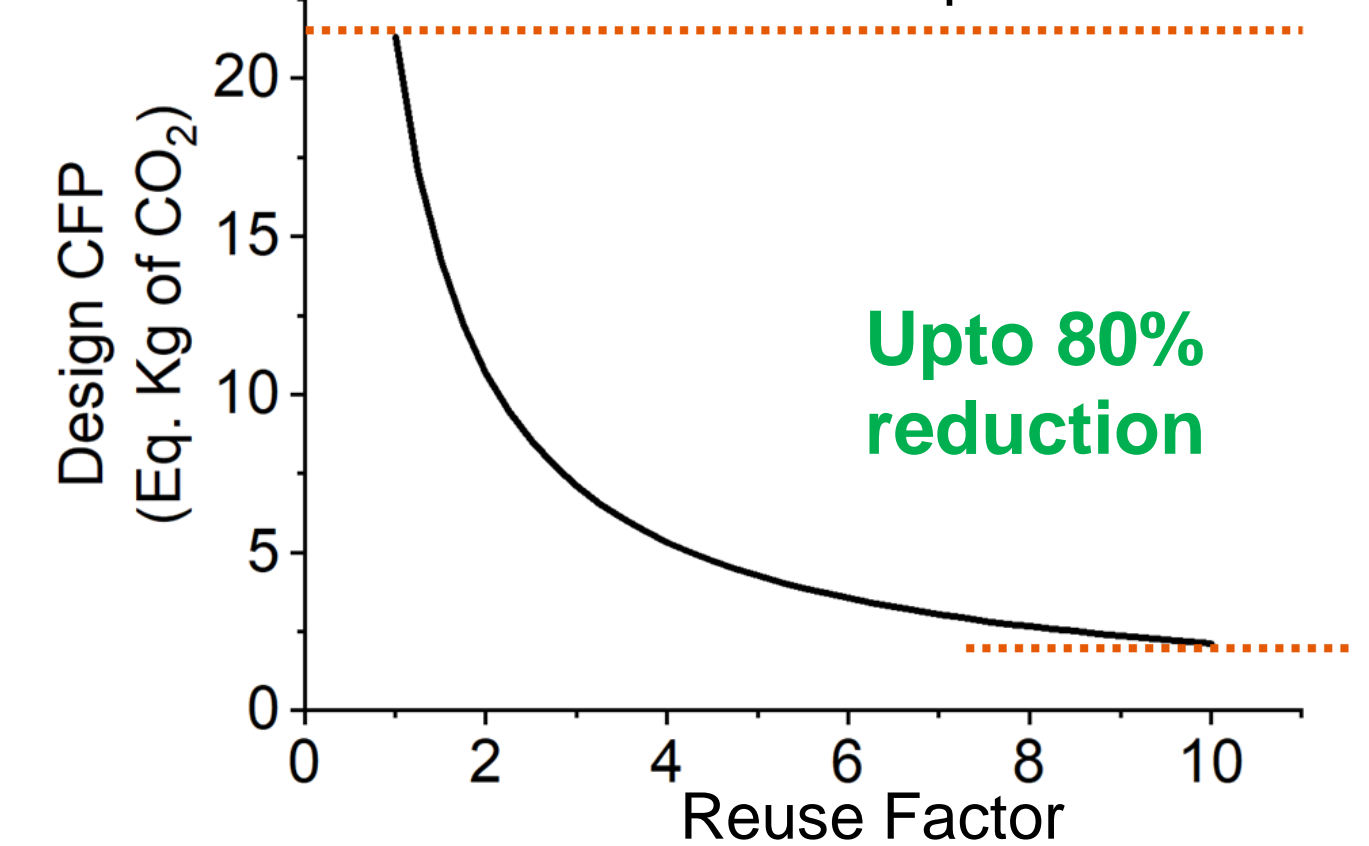


Key results and conclusion

- 40%** CFP reduction with **chiplet disaggregation**
- 36%** CFP reduction with **mix and match of technology nodes**
- Up to **80%** design CFP reduction with increased chiplet **reuse**



- ECO-CHIP analyzes CFP of **heterogeneous system**
- Advanced heterogeneous **packaging architecture** CFP overheads modeled
- Design CFP** modeled



Open-source code

