ECO-CHIP: Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI

Chetan Choppali Sudarshan, Nikhil Matkar, Sarma Vrudhula, Sachin S. Sapatnekar, Vidya A. Chhabria

HPCA 2024

Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- ECO-CHIP
  - HI Pathway to sustainability
  - Framework
  - ECO-CHIP carbon footprint models
  - Key takeaways
- Conclusion

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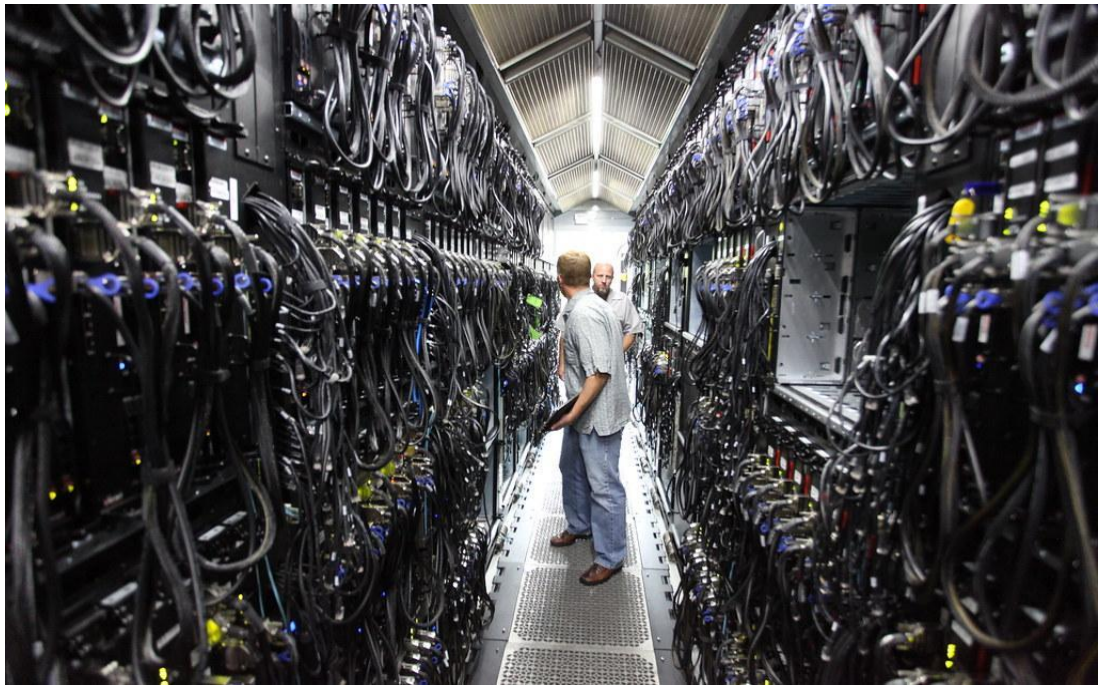
Information and Computing Technology (ICT)

Data Center and Networks



User devices

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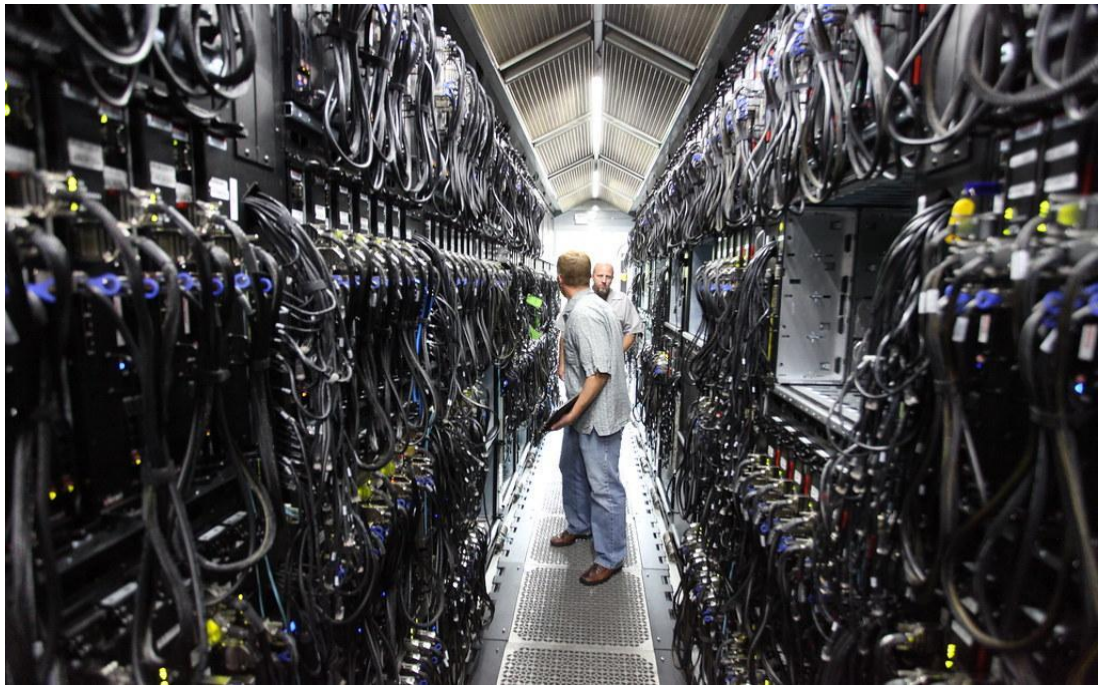

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- Need for sector-wide regulations

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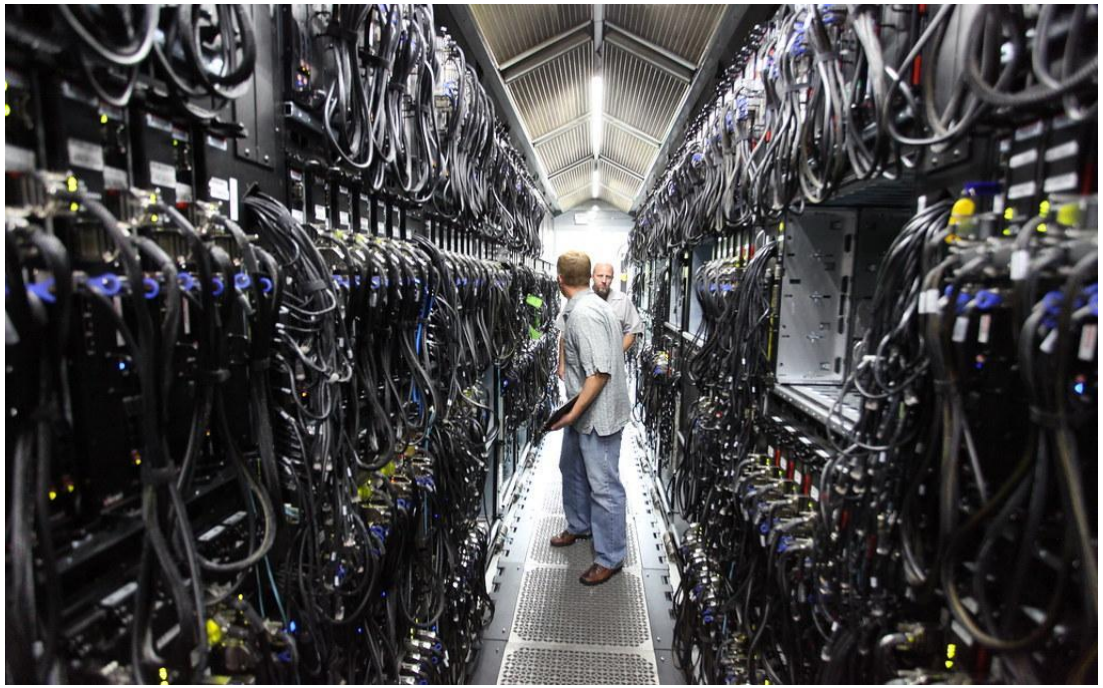

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Industry and government interest

PRESS RELEASE
July 21, 2020

Apple commits to be 100 percent carbon neutral for its supply chain and products by 2030

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U.S. National Science Foundation

Find Funding & Apply Manage Your Award Focu

Home / Funding at NSF / Funding Search / Design for Environmental Sustainability in Computing (DESC)

Important information for proposers
All proposals must be submitted in accordance with the requirements specified in this funding opportunity and in the NSF Proposal & Award Policies & Procedures Guide (PAPPG) that is in effect..

Supports foundational research addressing the substantial environmental impacts of computing. Projects should surpass studies of energy efficiency alone, pursuing dramatic improvements to overall sustainability.

NSF 22-060

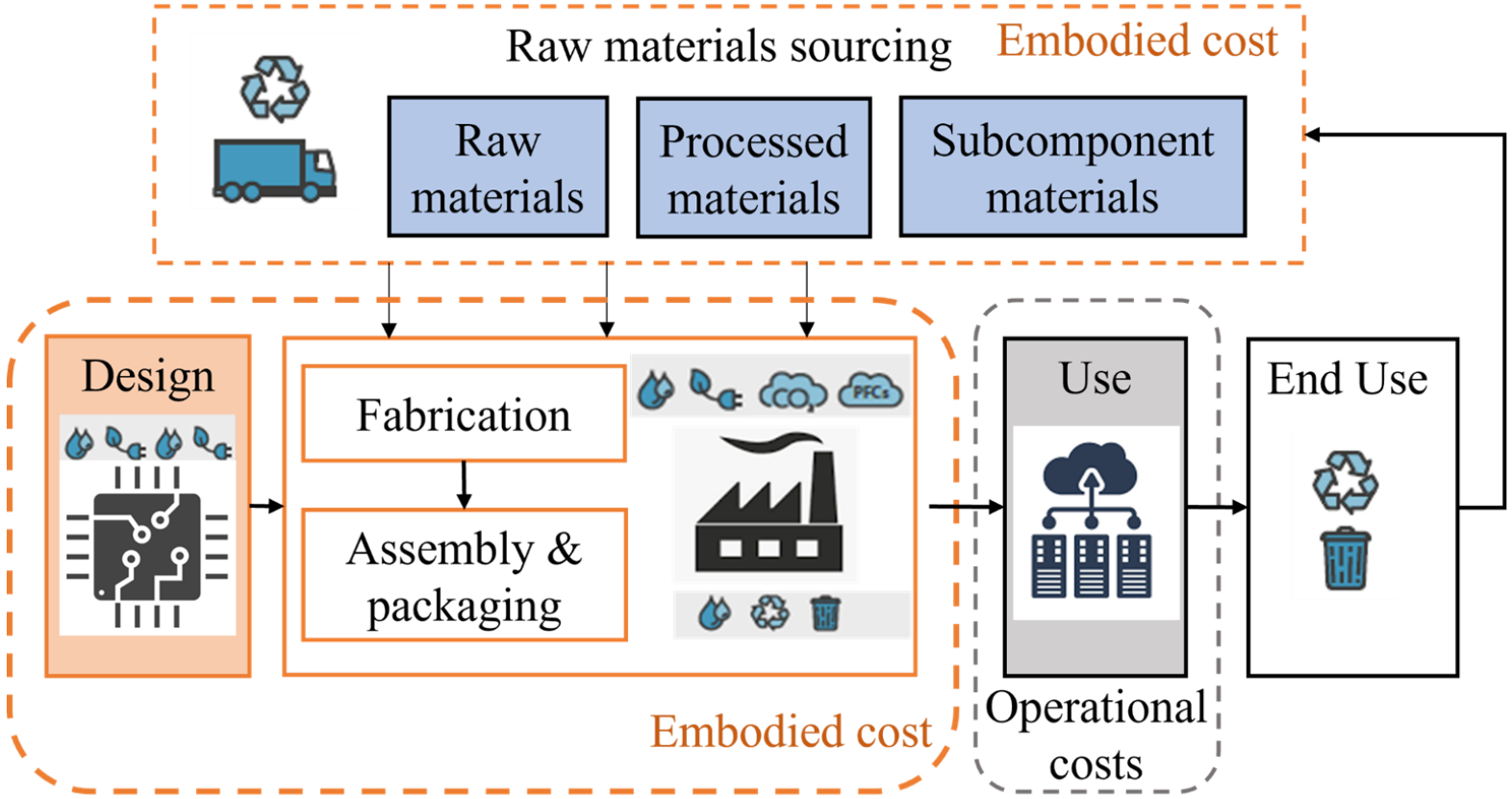
Dear Colleague Letter: Design for Sustainability in Computing

March 15, 2022

Dear Colleagues:

Environmental impacts of computing technologies extend well beyond their energy consumption and require a holistic focus on broader sustainability. Negative impacts of greenhouse gas emissions, depletion of rare earth elements, and e-waste are exacerbated by the proliferation of computing throughout society and treatment of computing systems as disposable commodities with planned obsolescence. Furthermore, environmental concerns range from the better-known carbon footprint from energy consumption (e.g., cloud) to equally important concerns of embodied carbon[1], generation of methane, carcinogens, volatile organic compounds, and eutrophication, among others. Widespread use of compute intensive techniques (e.g., blockchain and artificial intelligence), handling and moving massive amounts of data, the rollout of next generation

Silicon lifecycle and sources of carbon



Silicon lifecycle and sources of carbon

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  - Design CFP
  - Manufacturing and packaging CFP
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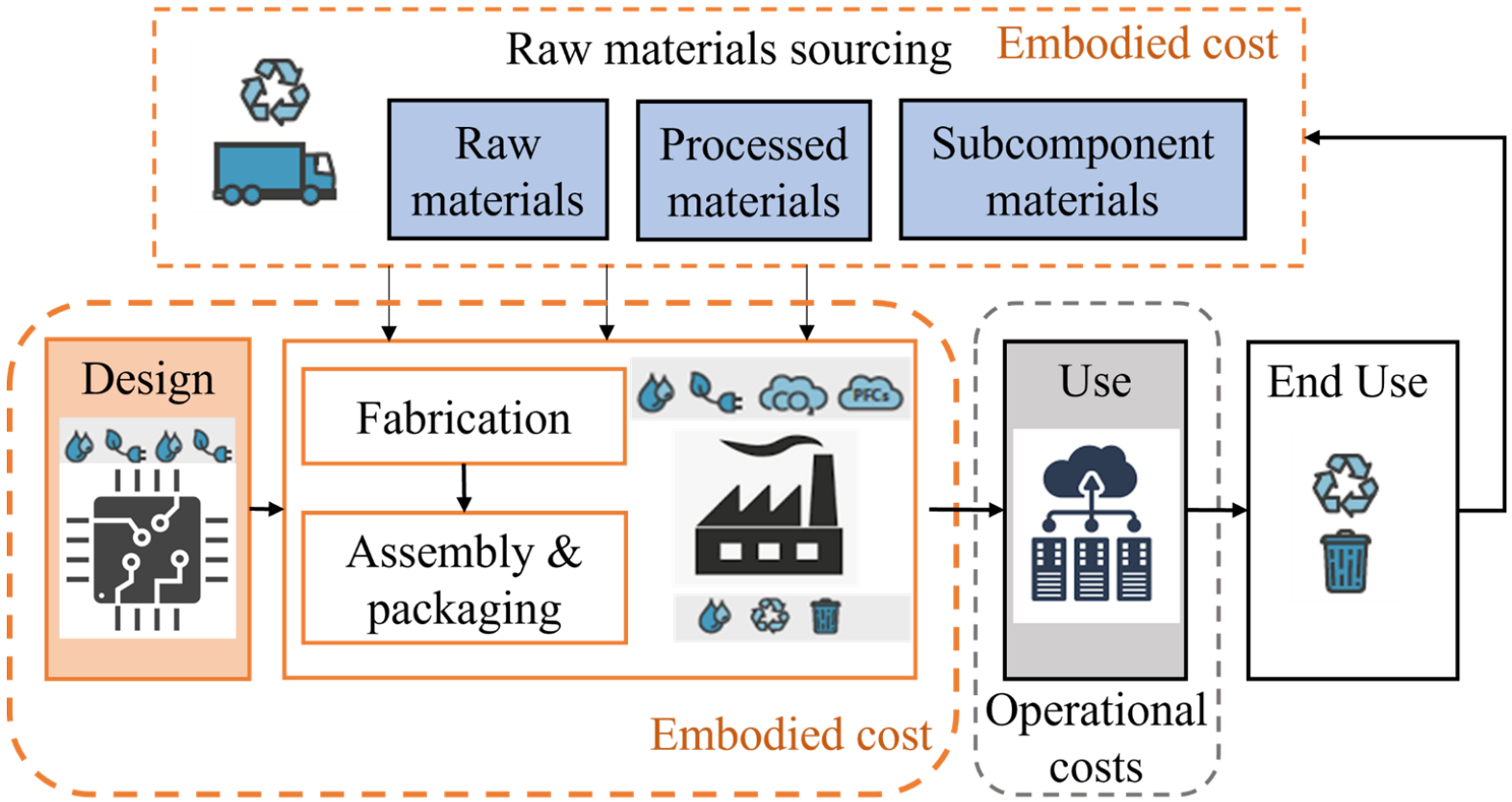
  - CFP from end-user



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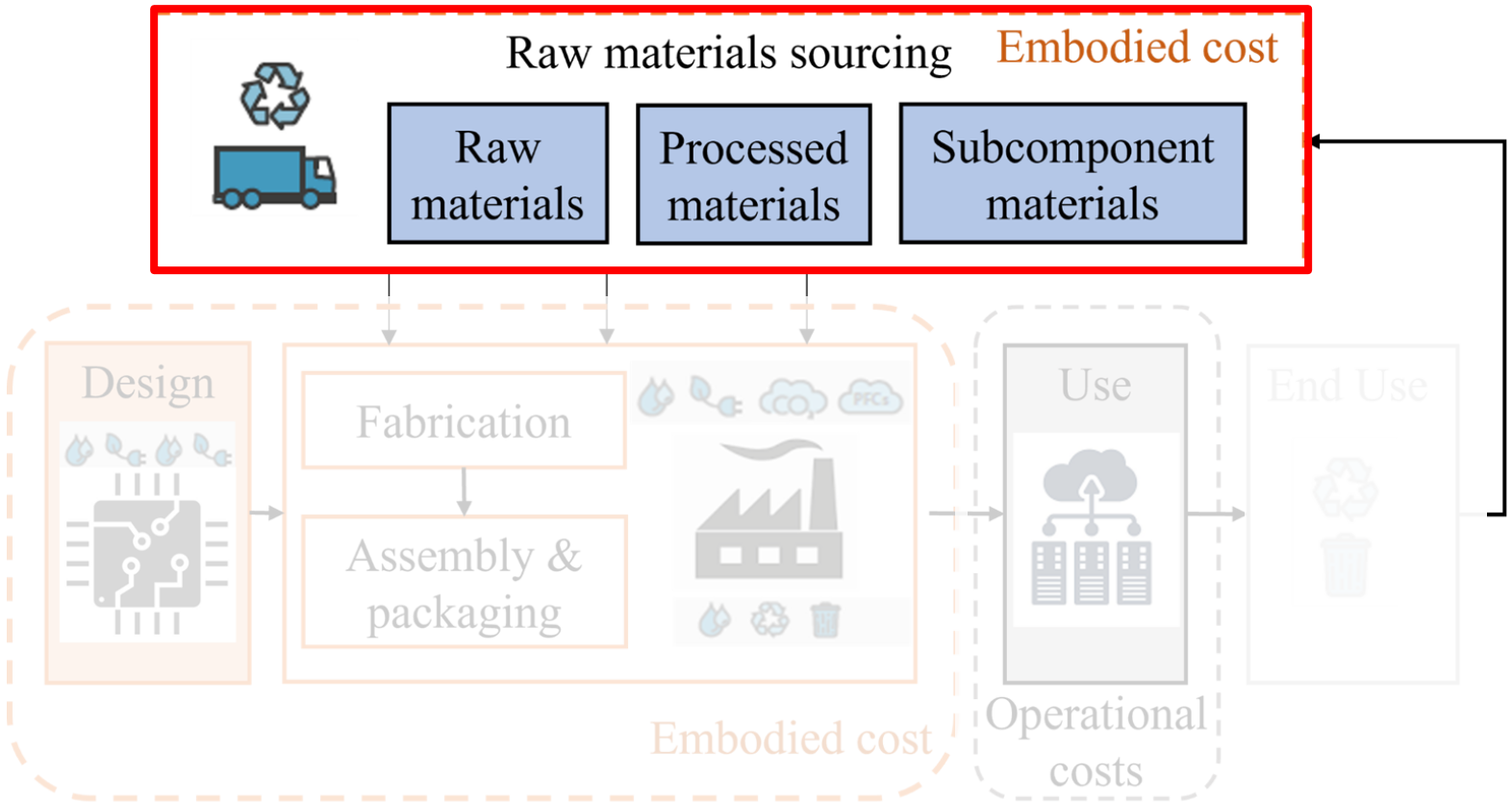

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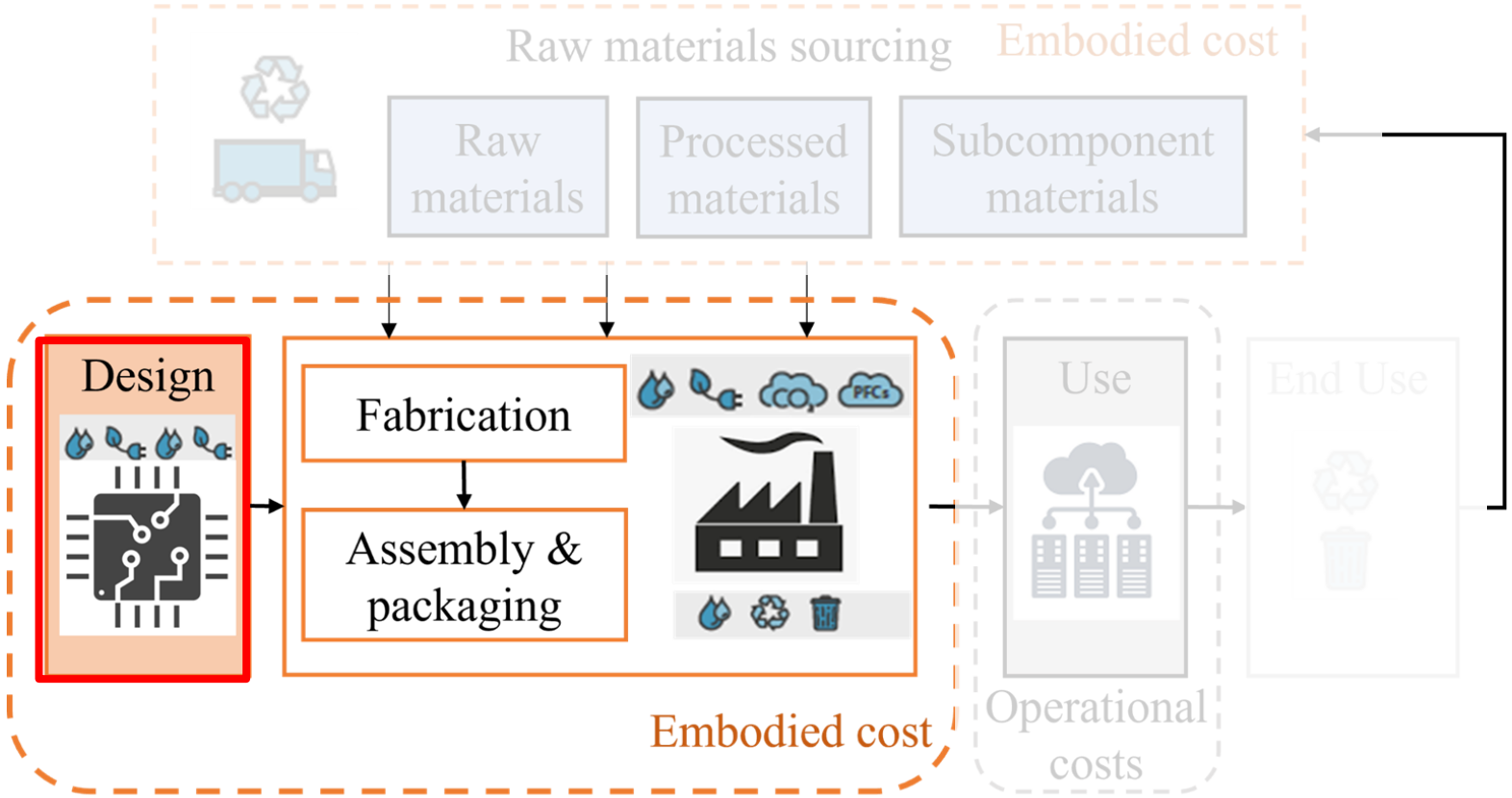

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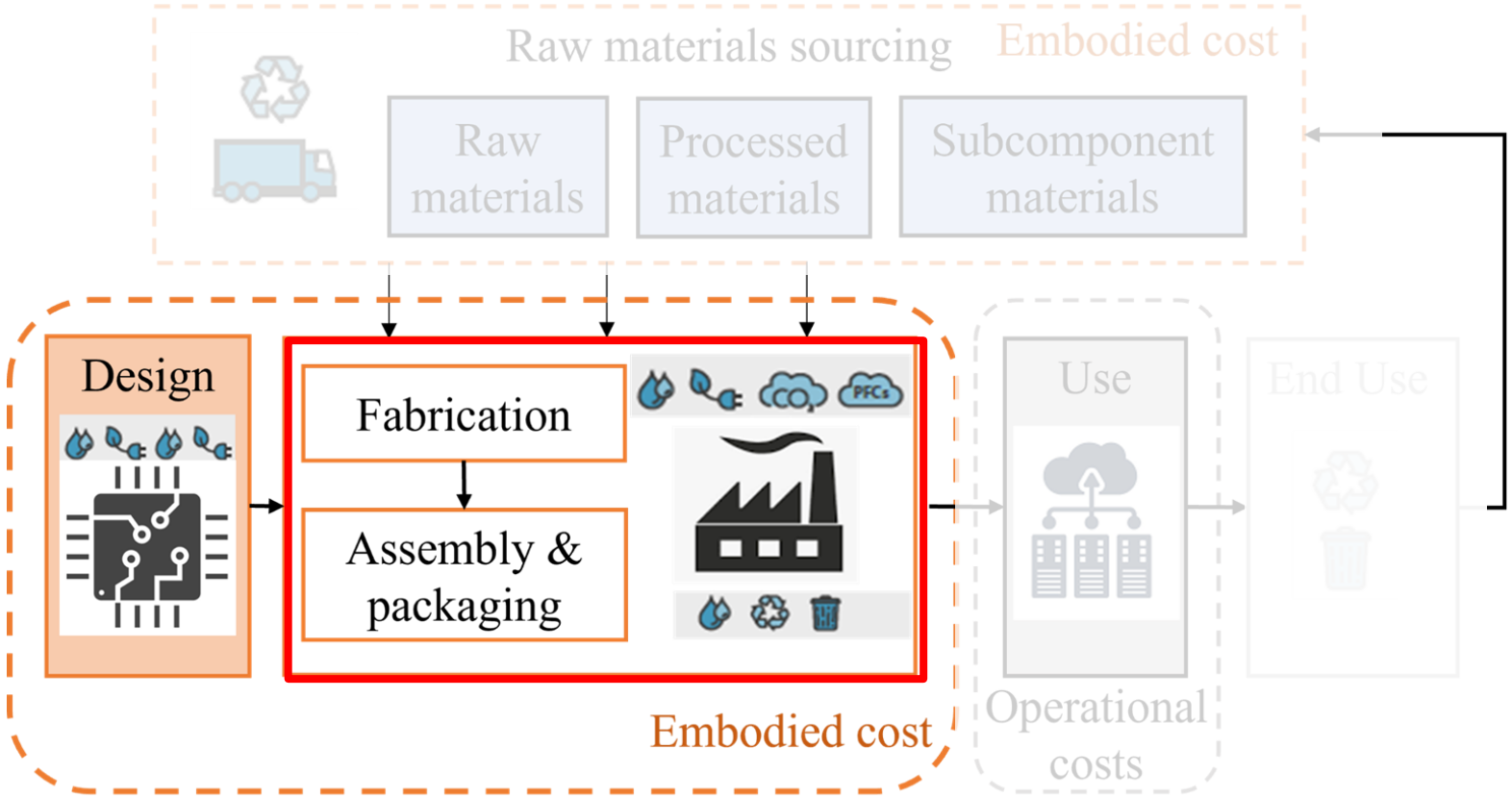

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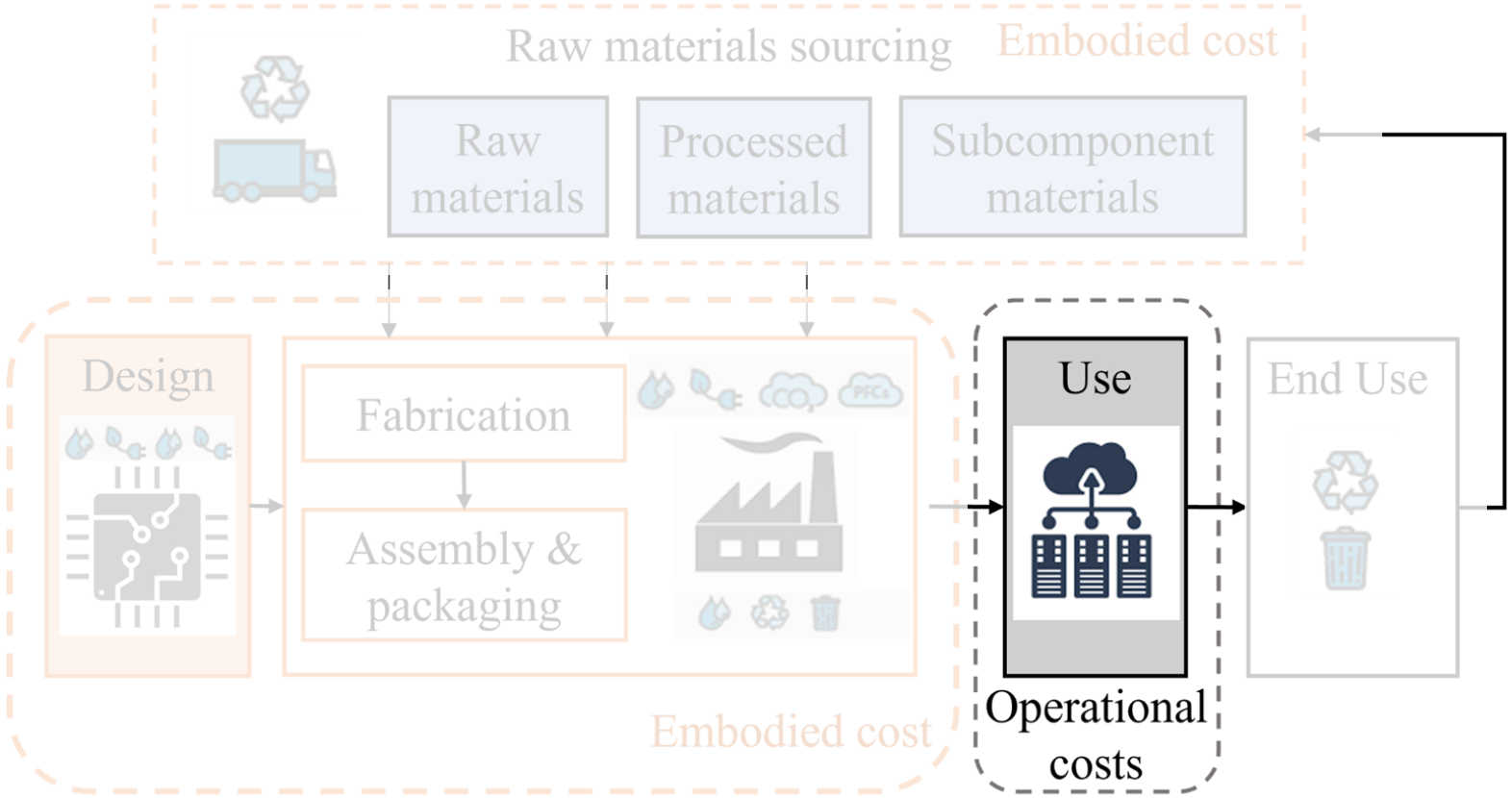

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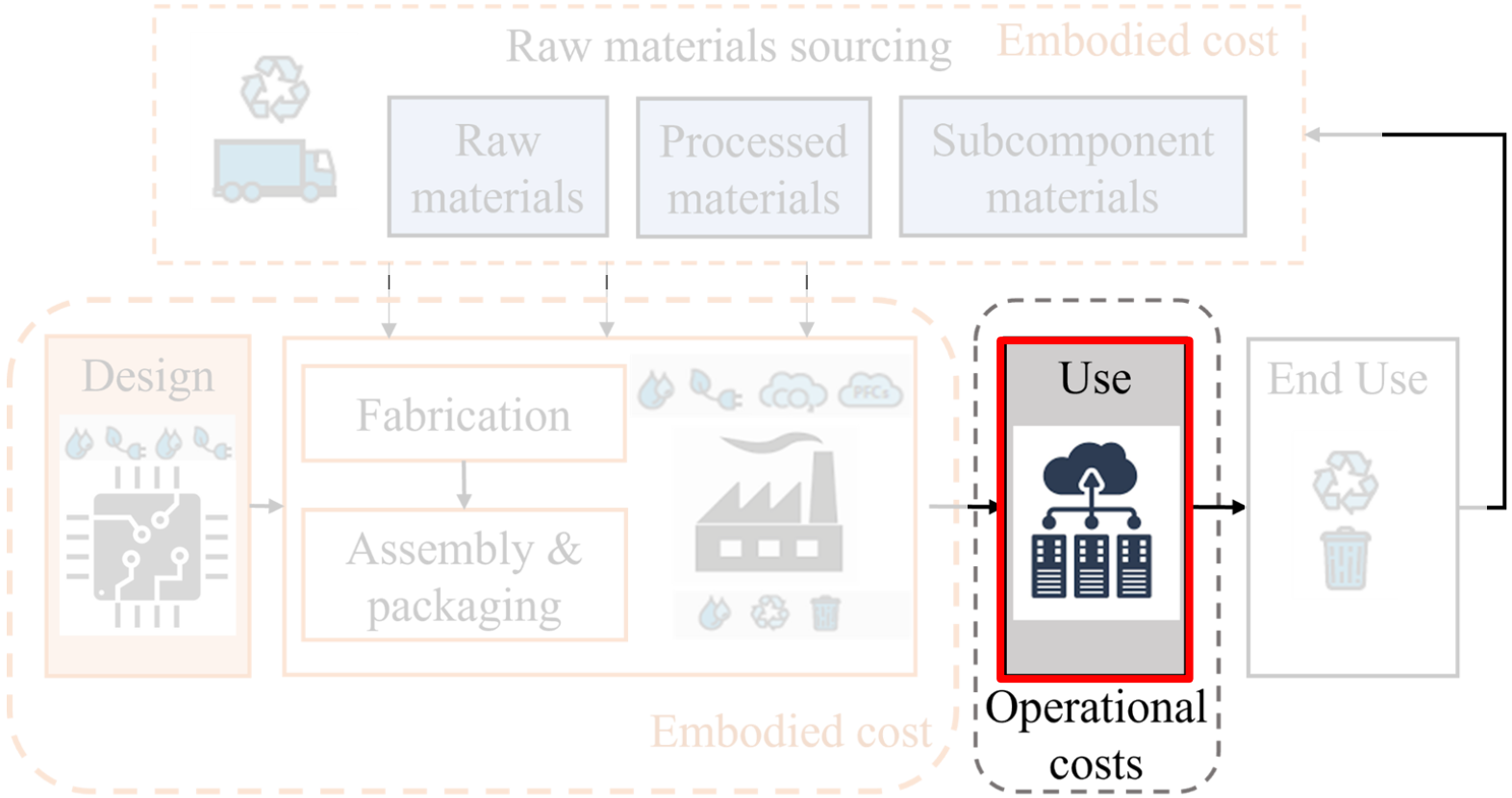

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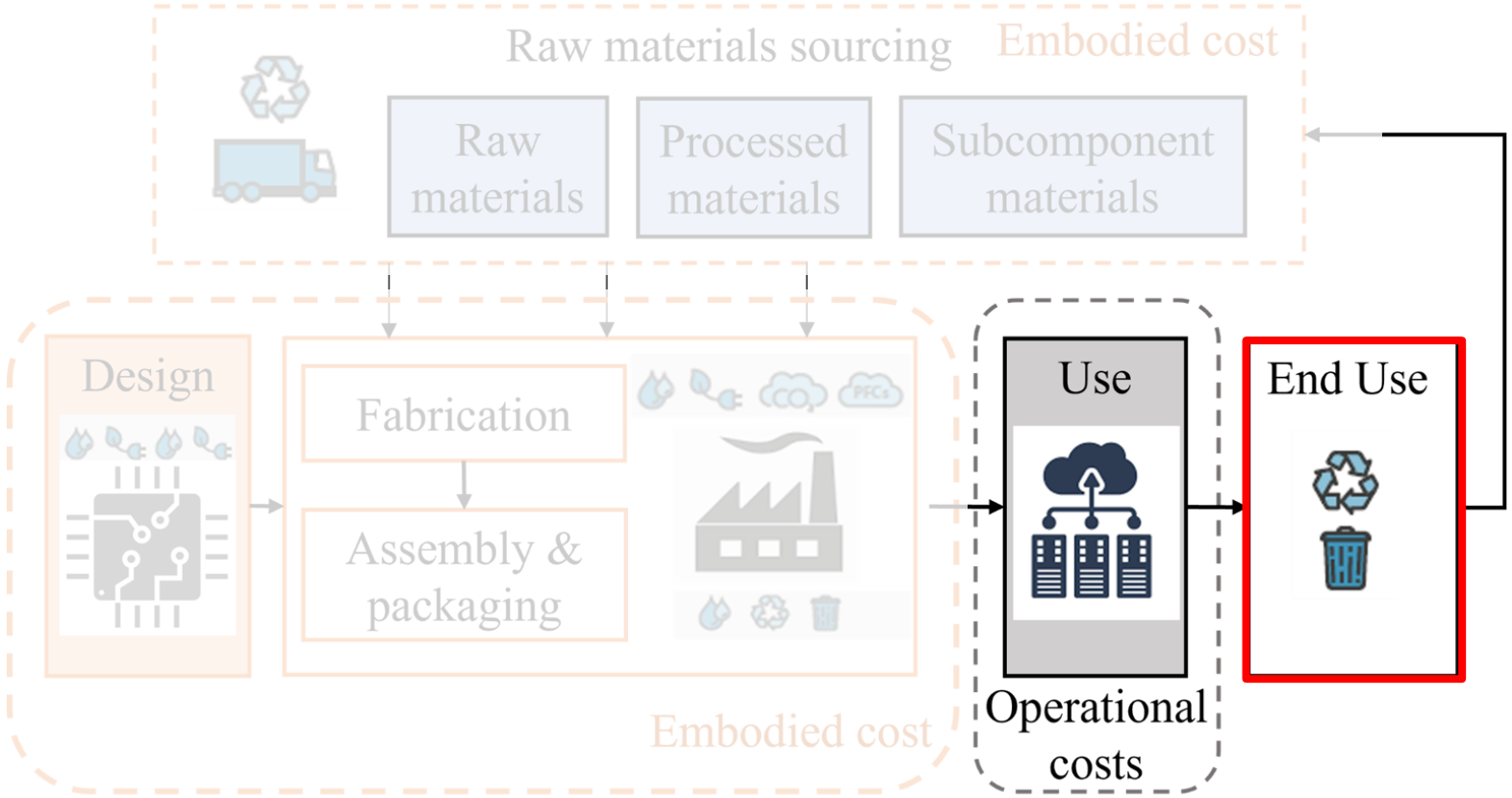
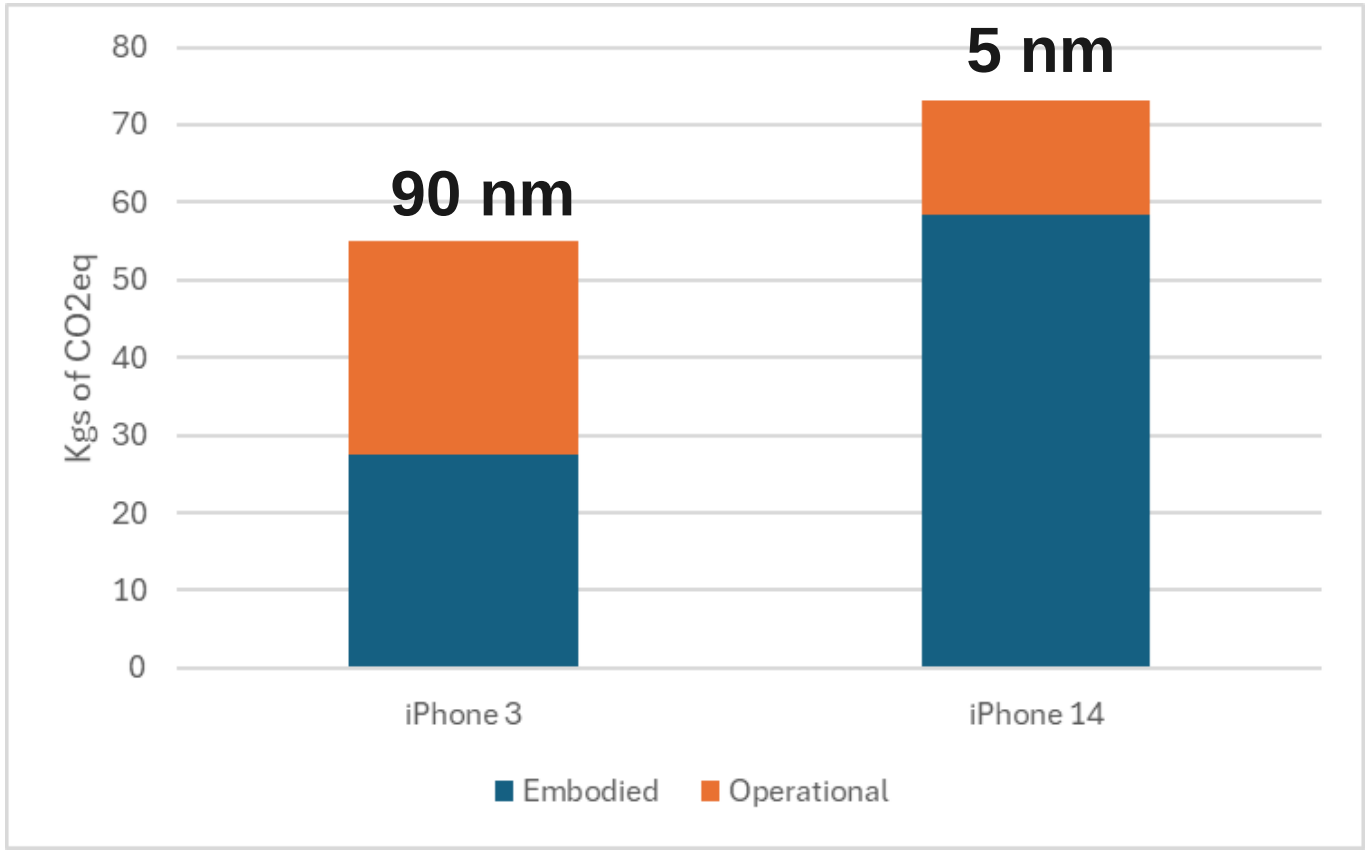


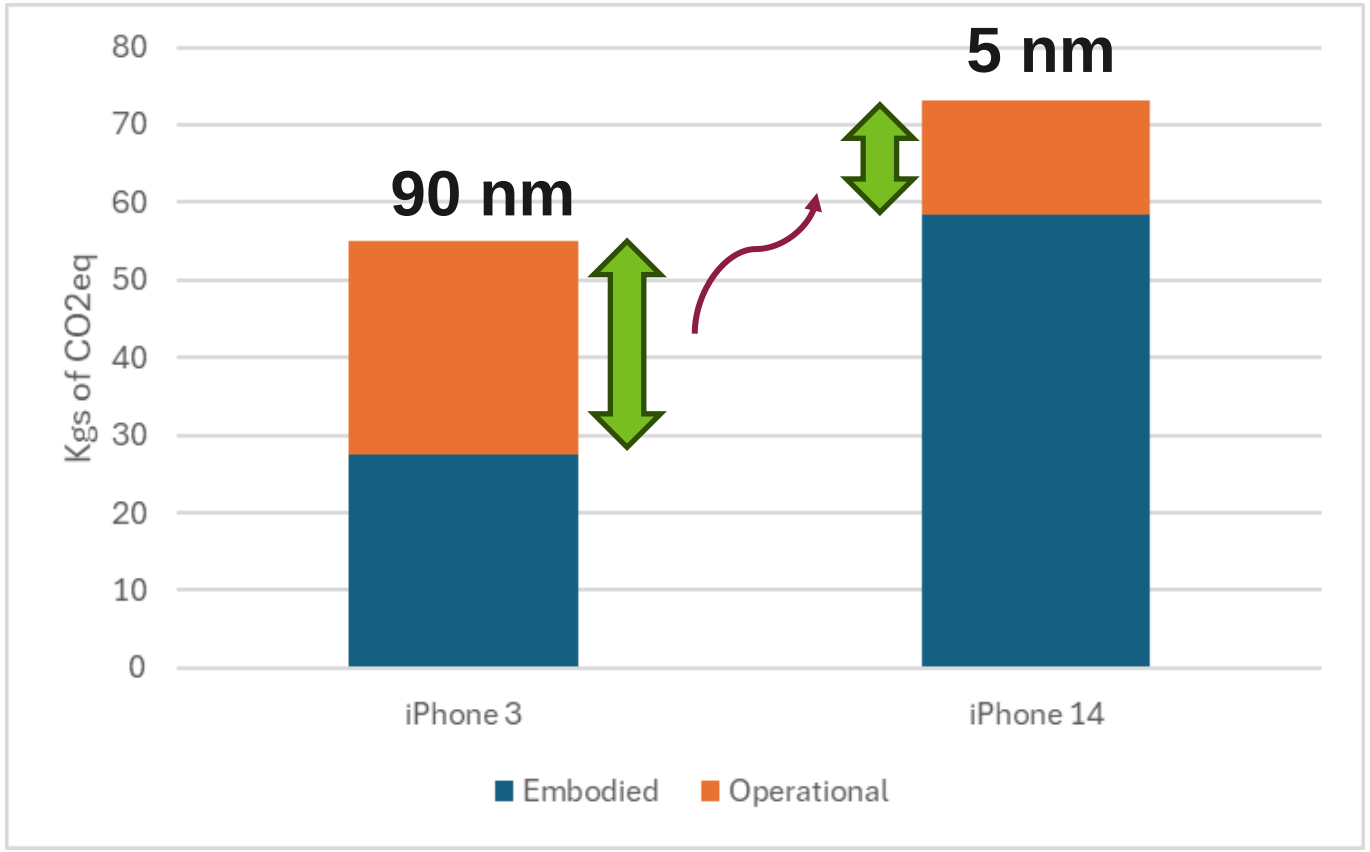
Challenges and demands



Source : Apple sustainability reports

Challenges and demands

- Efficiency optimization
  - Operational CFP drops 46%
- Rising embodied carbon
  - Embodied CFP increases 110%



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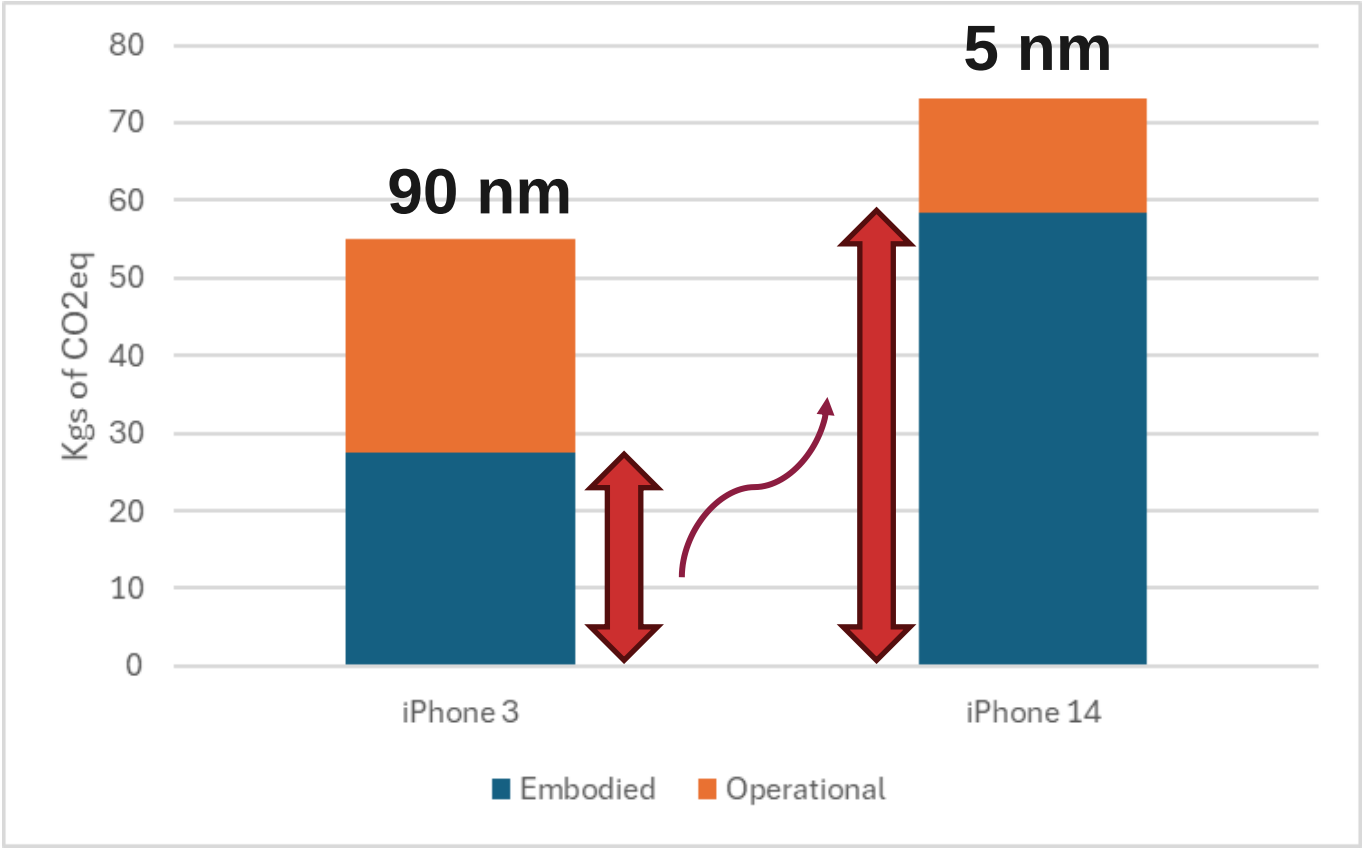

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- Carbon-aware exploration framework
- Architectural model estimating embodied carbon
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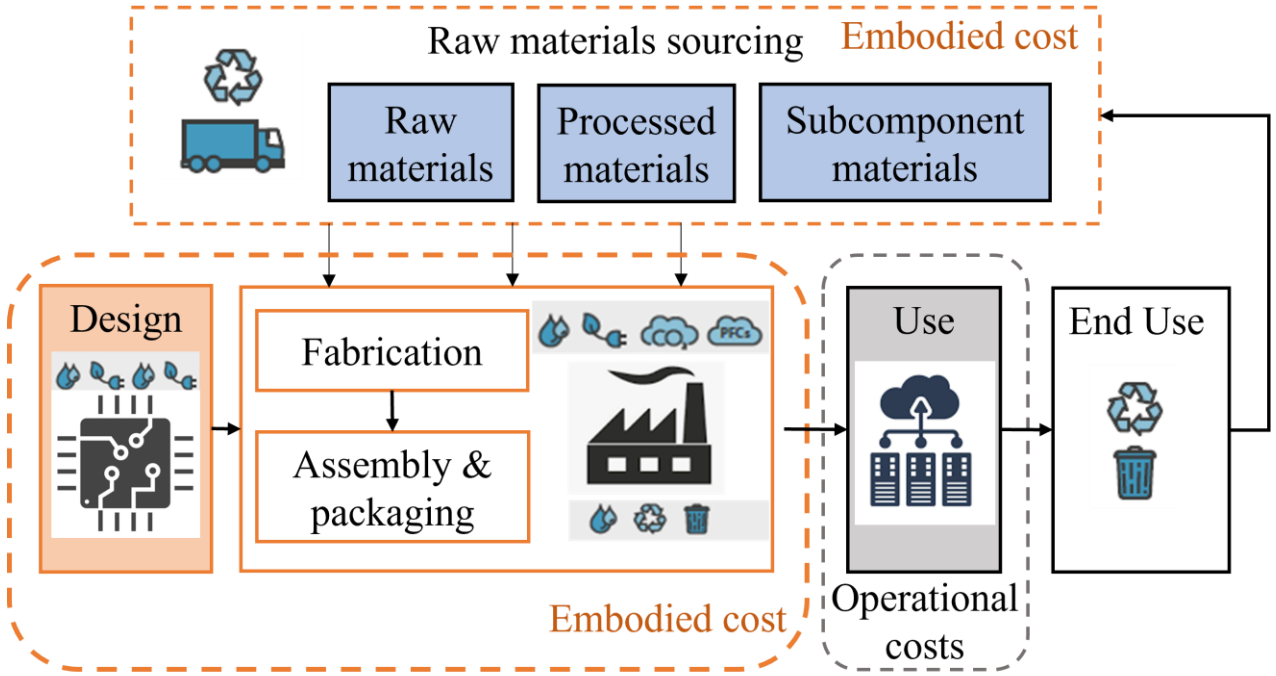

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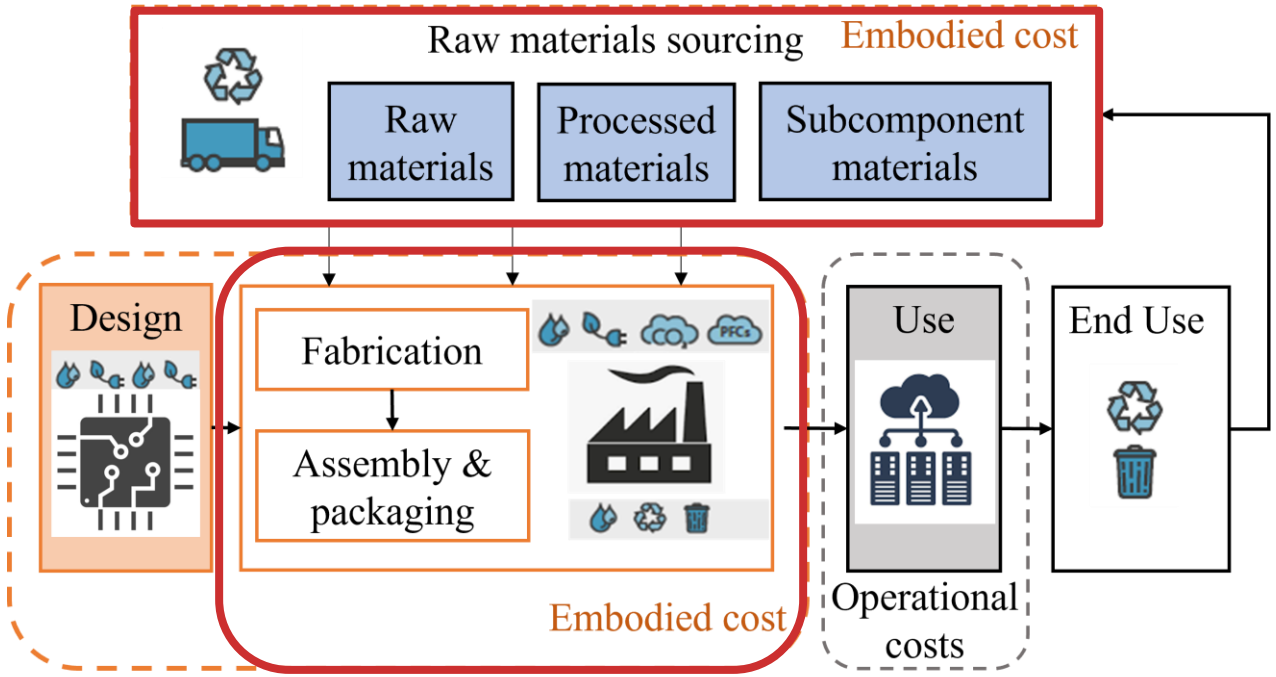

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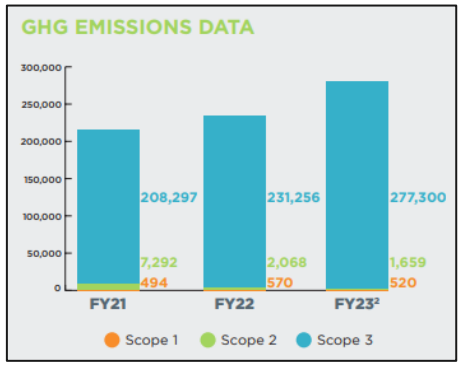

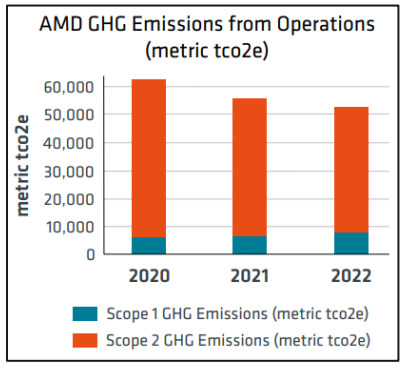

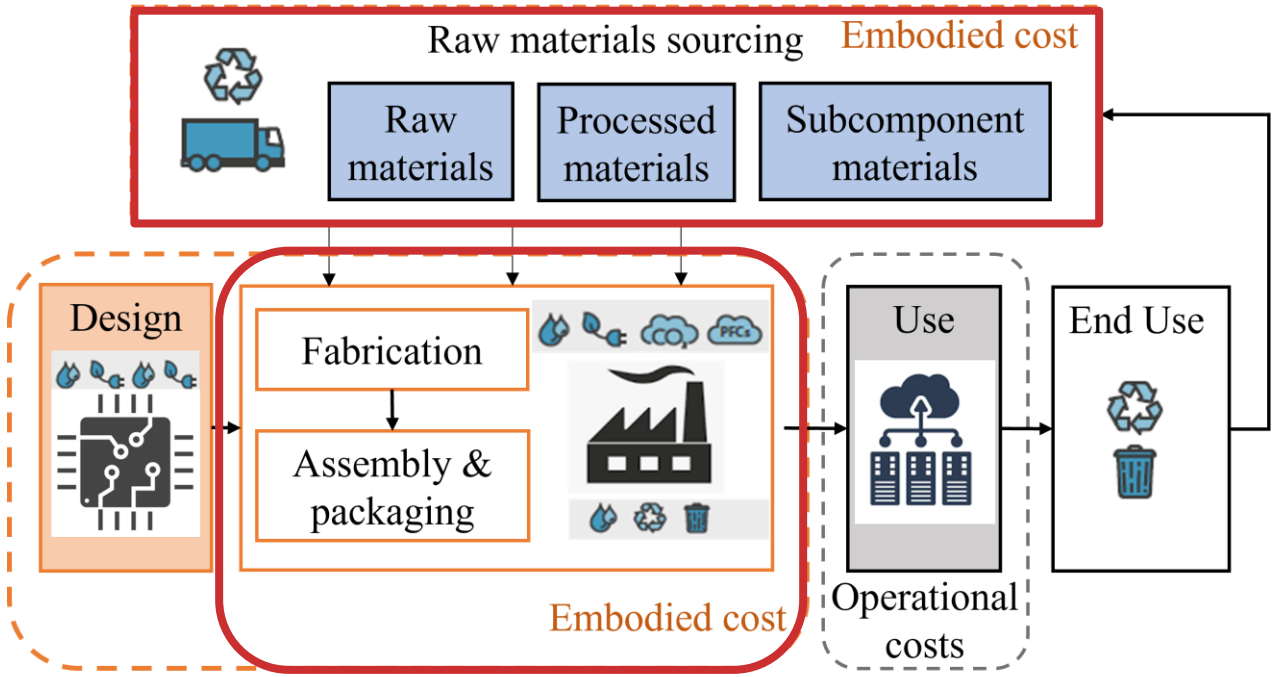

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This work: Our approach to sustainable computing

3R’s for sustainability

- Reduce
- Reuse
- Recycle

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Our approach

Heterogeneous system sustainability (ECO-CHIP)

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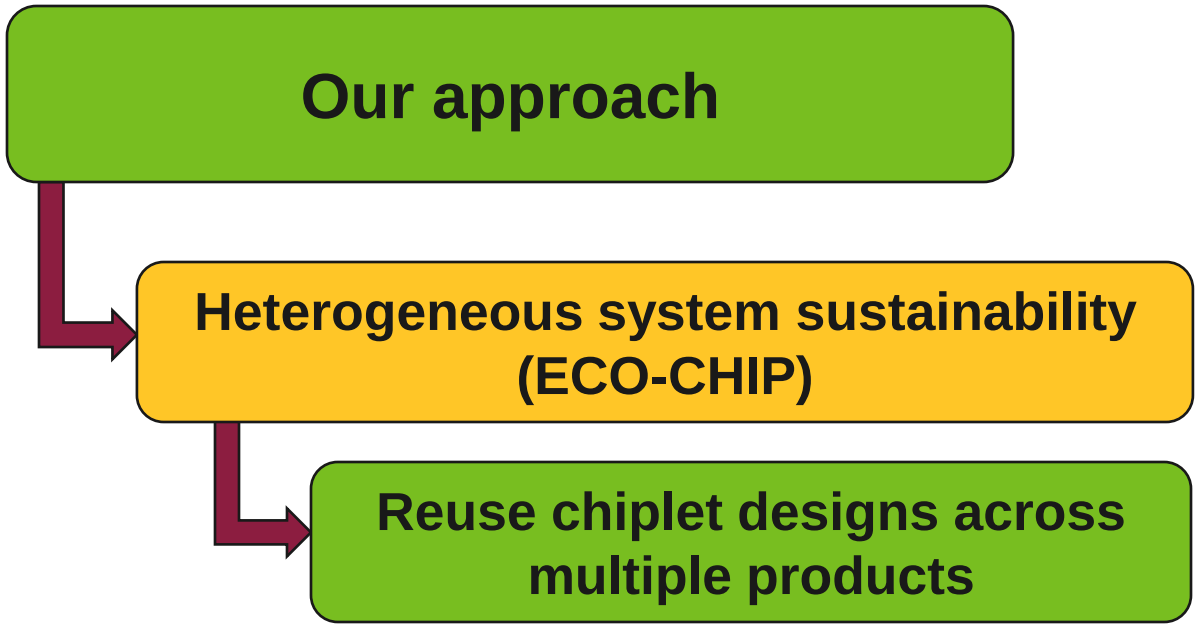

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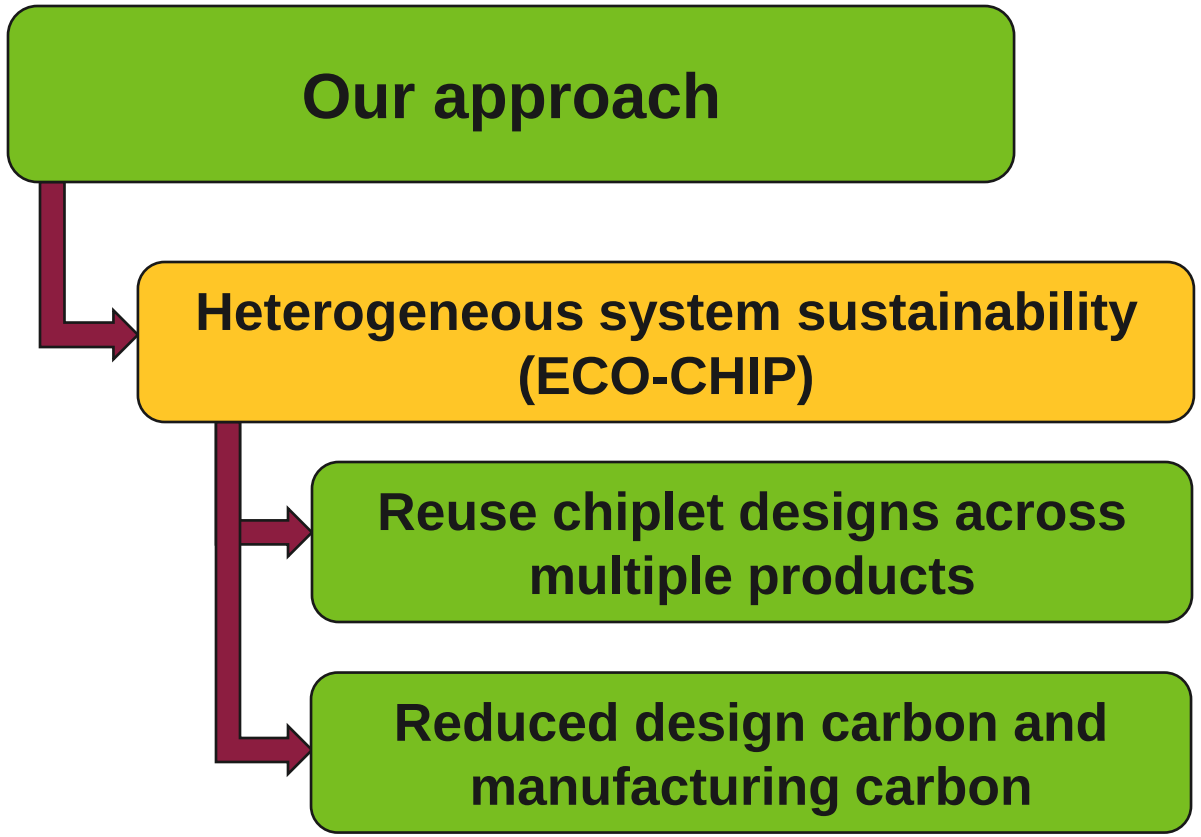

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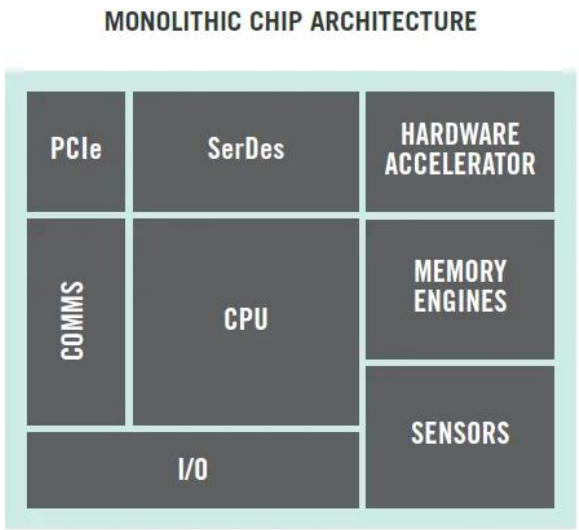
Heterogeneous Integration (HI)

- Large SoCs are at reticle limit



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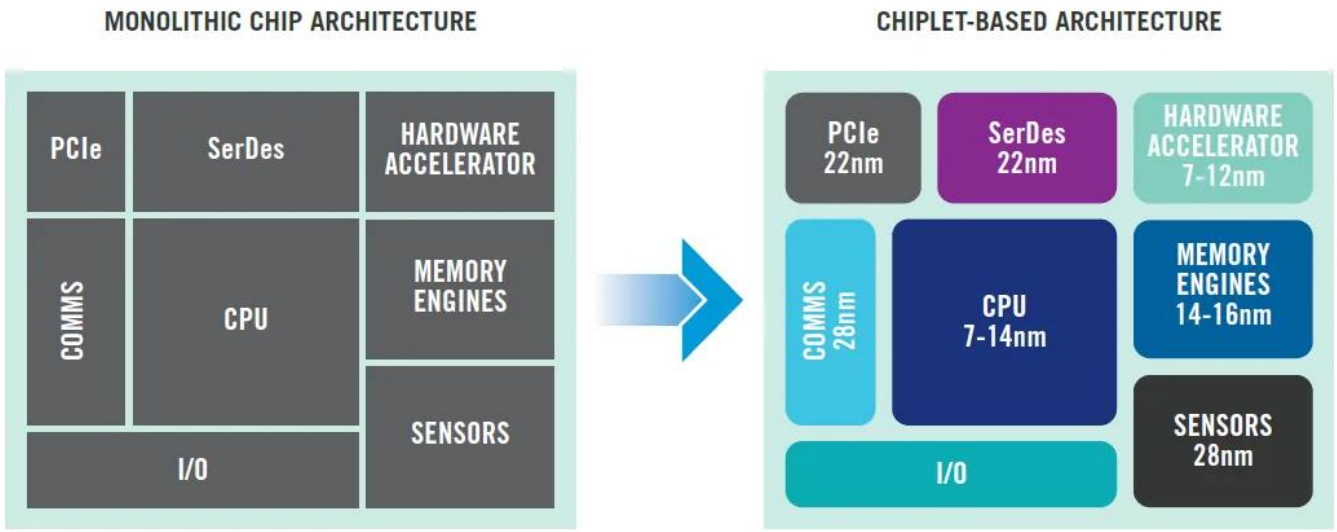

Source : Lawrence Lundy-Bryan FRSA, LinkedIn post

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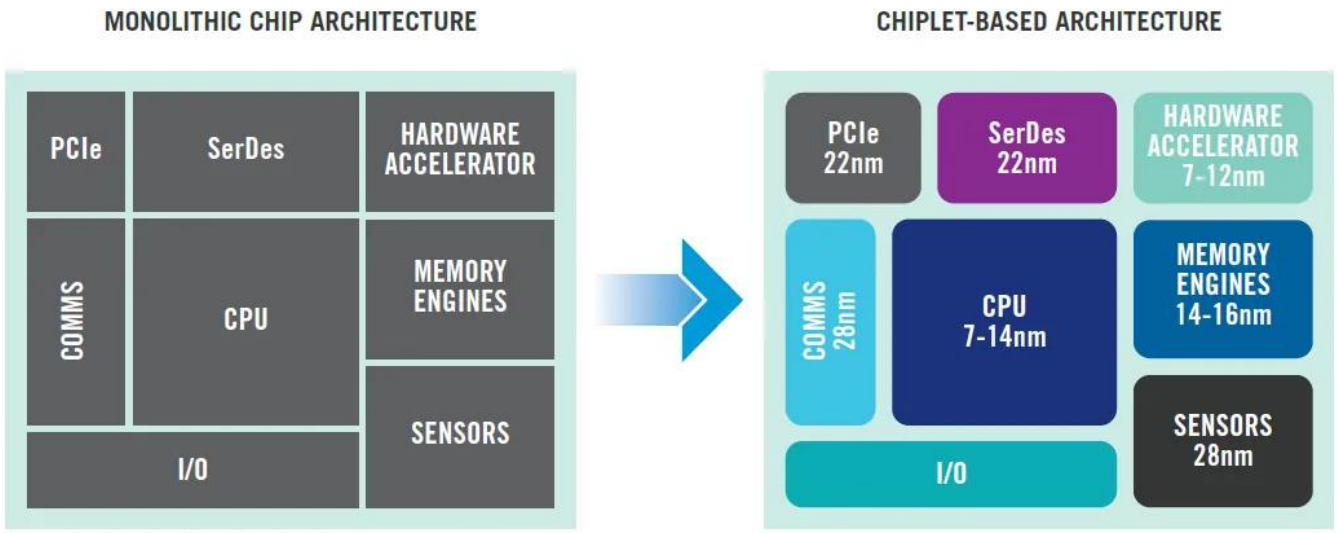
- The key enabler for heterogeneous integration are advanced packaging techniques



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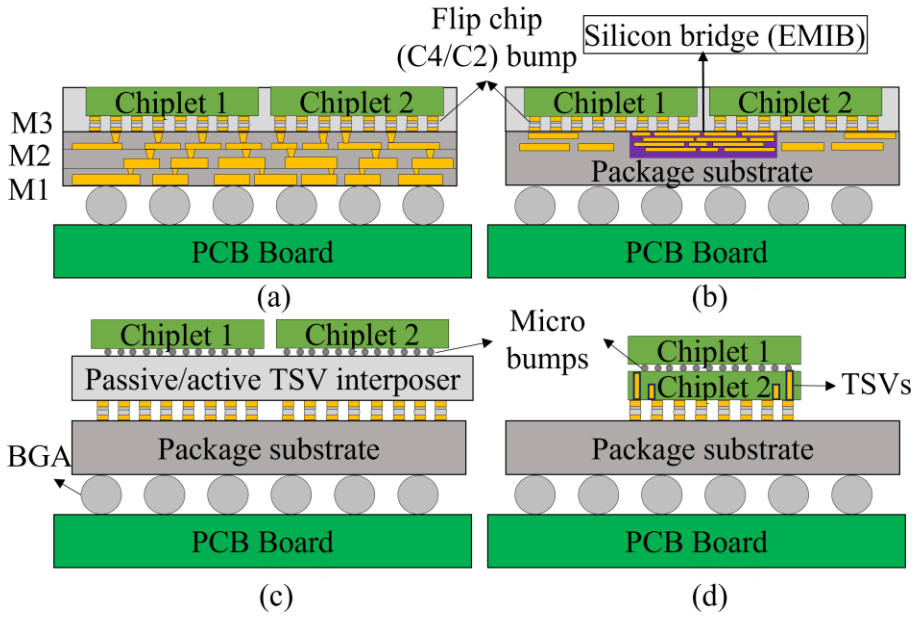

HI as a path towards sustainable computing

Sustainable Computing

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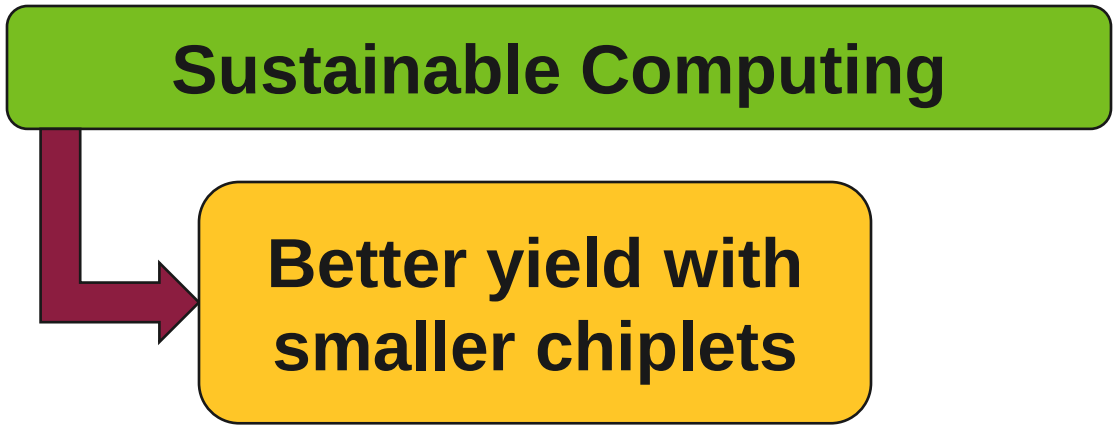
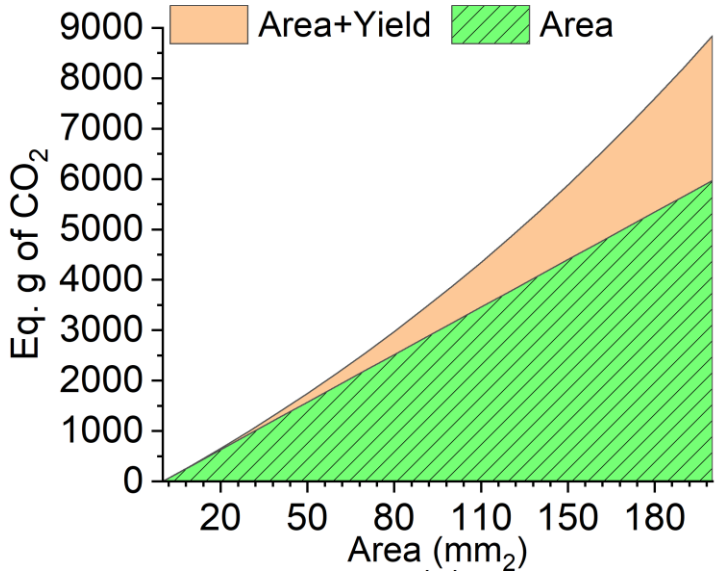
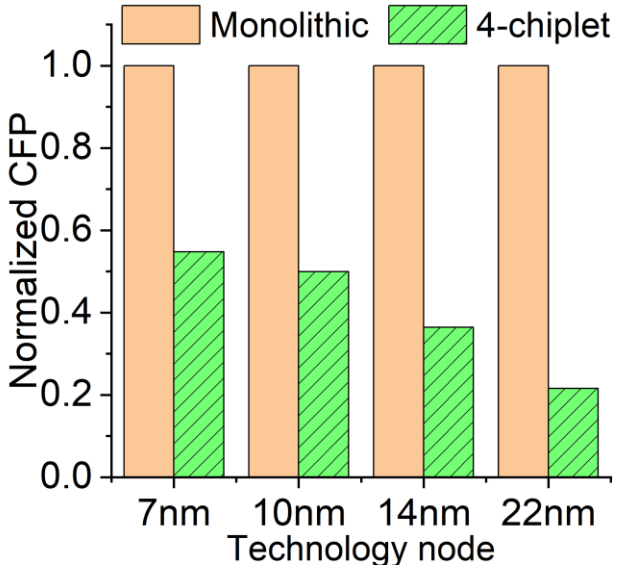


HI as a path towards sustainable computing

Sustainable Computing

Better yield with smaller chiplets





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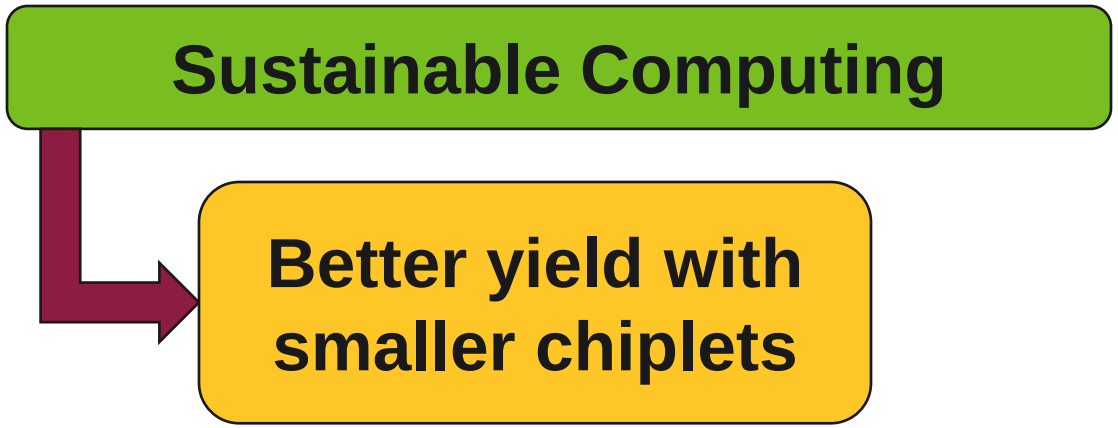

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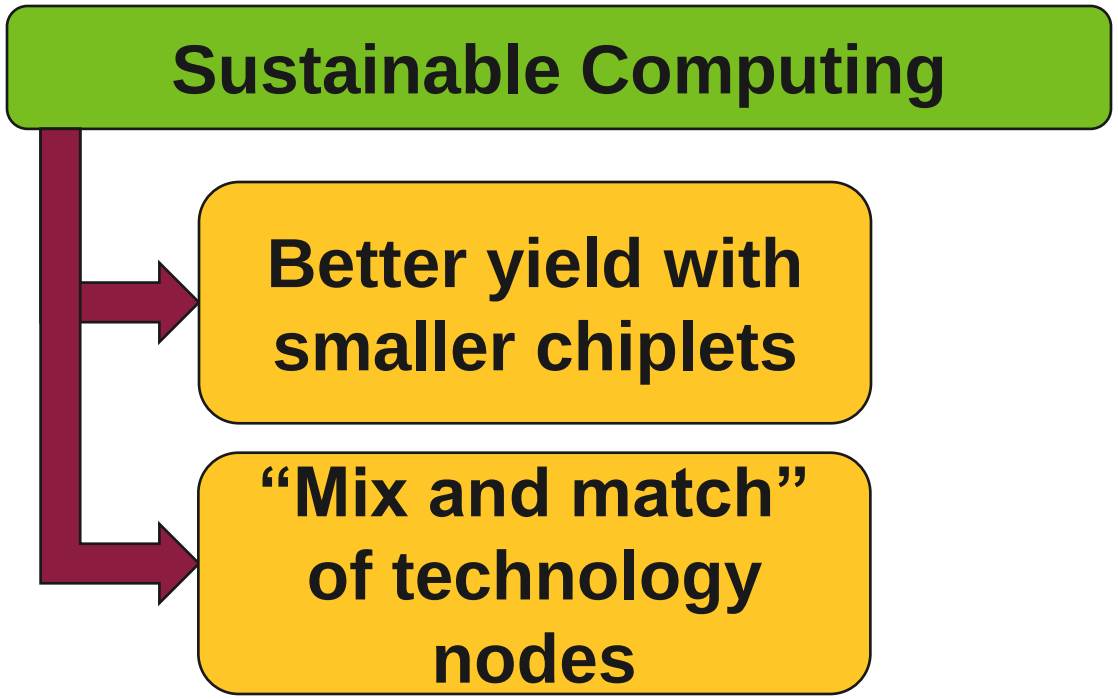
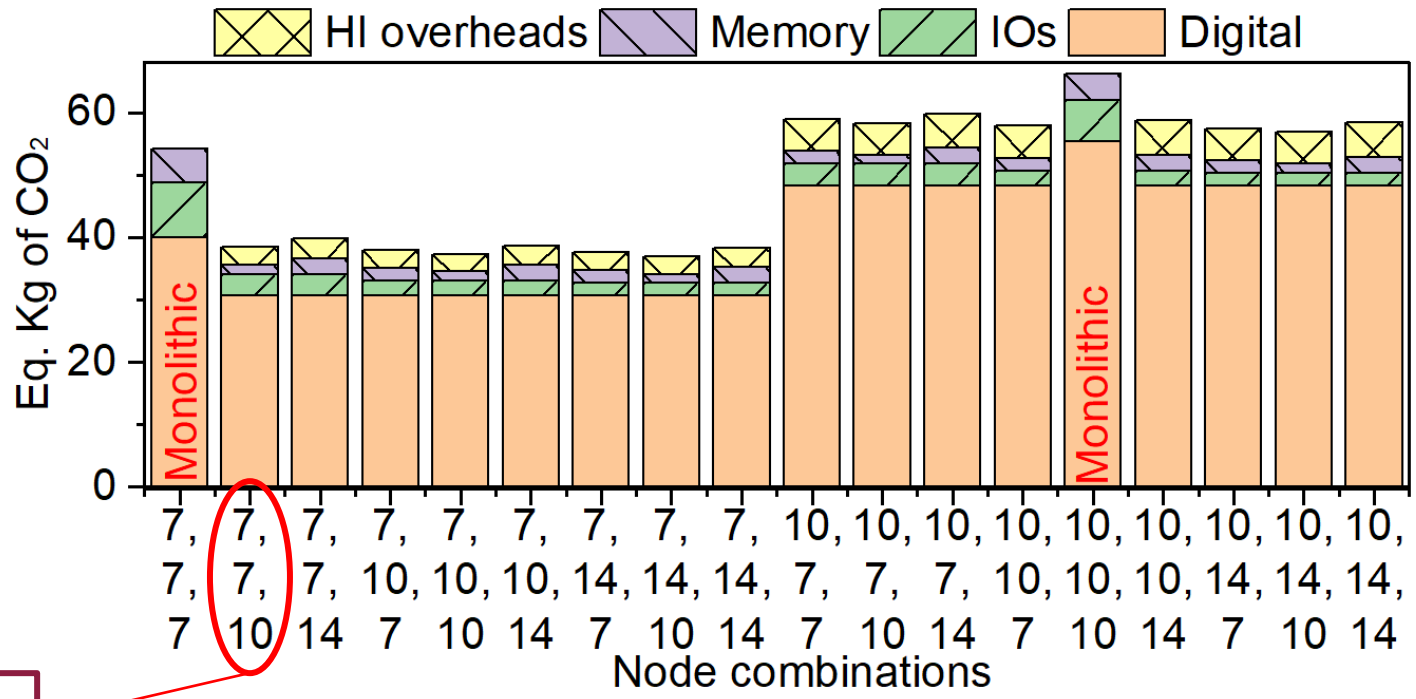


HI as a path towards sustainable computing

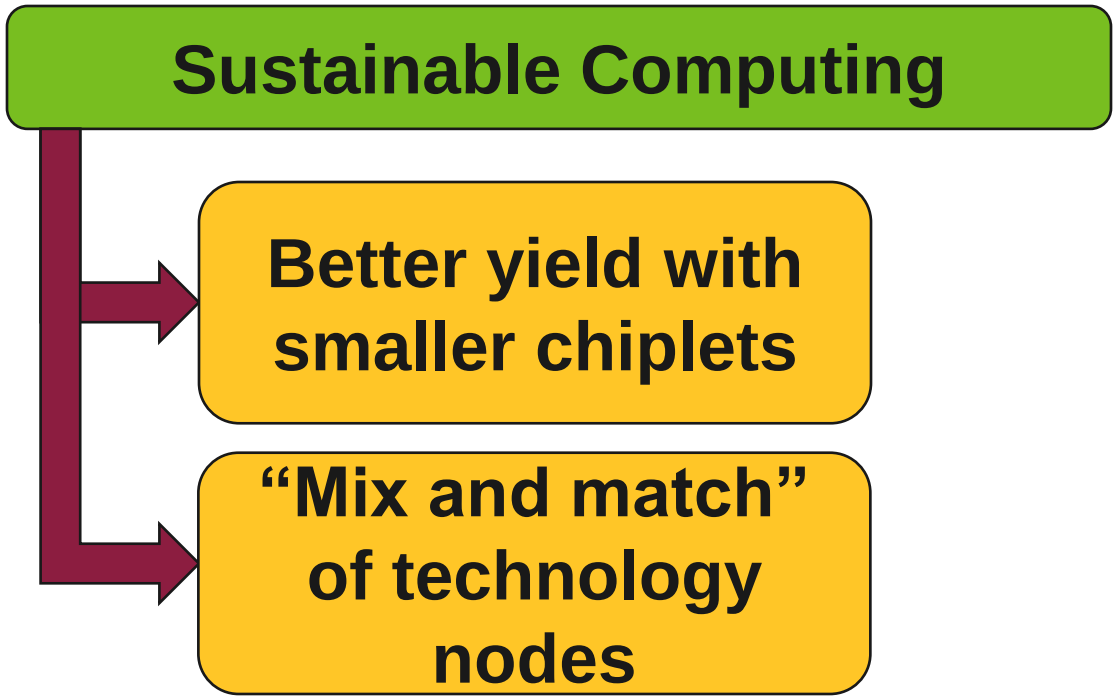
Sustainable Computing

- **Better yield with smaller chiplets**
- **"Mix and match" of technology nodes**



7,7,10 => 7nm Logic
7nm IOs
10nm Memory
7,7,7 => Monolithic on 7nm

HI as a path towards sustainable computing



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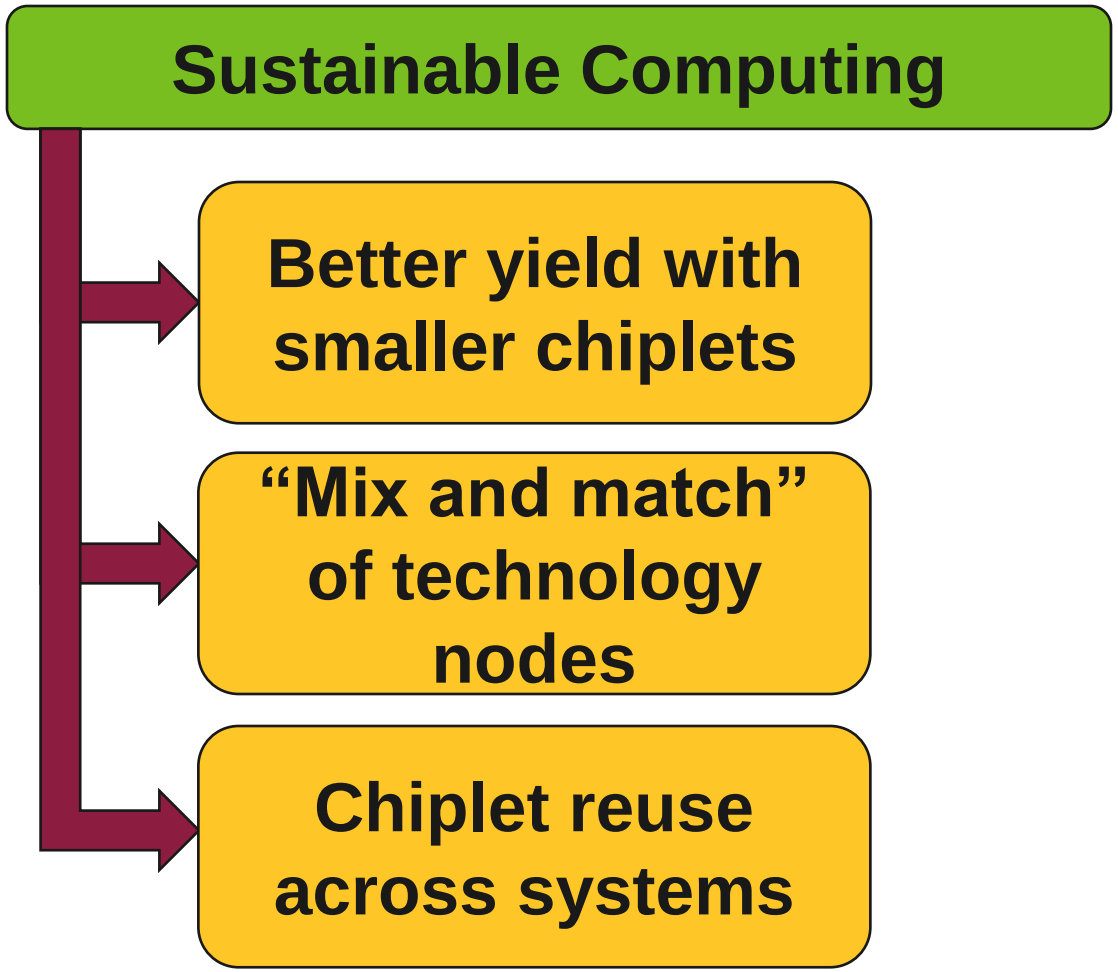

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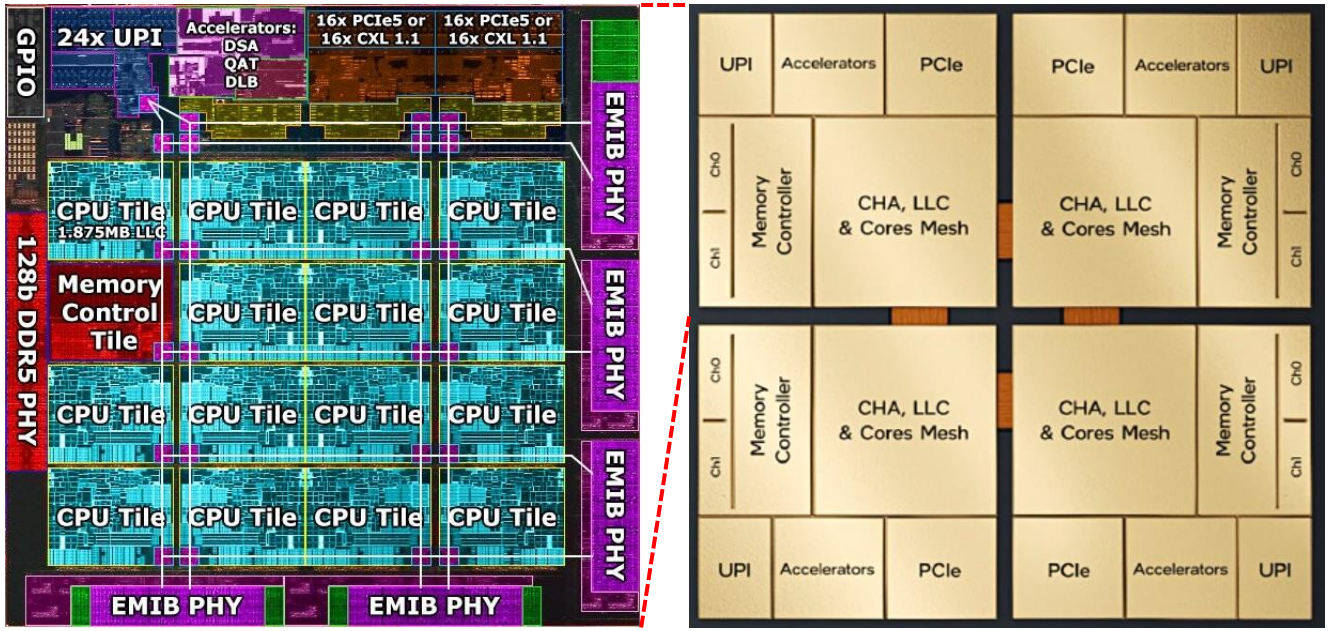
- **“Mix and match” of technology nodes**
- **Chiplet reuse across systems**



Source : Intel, Screenhacker

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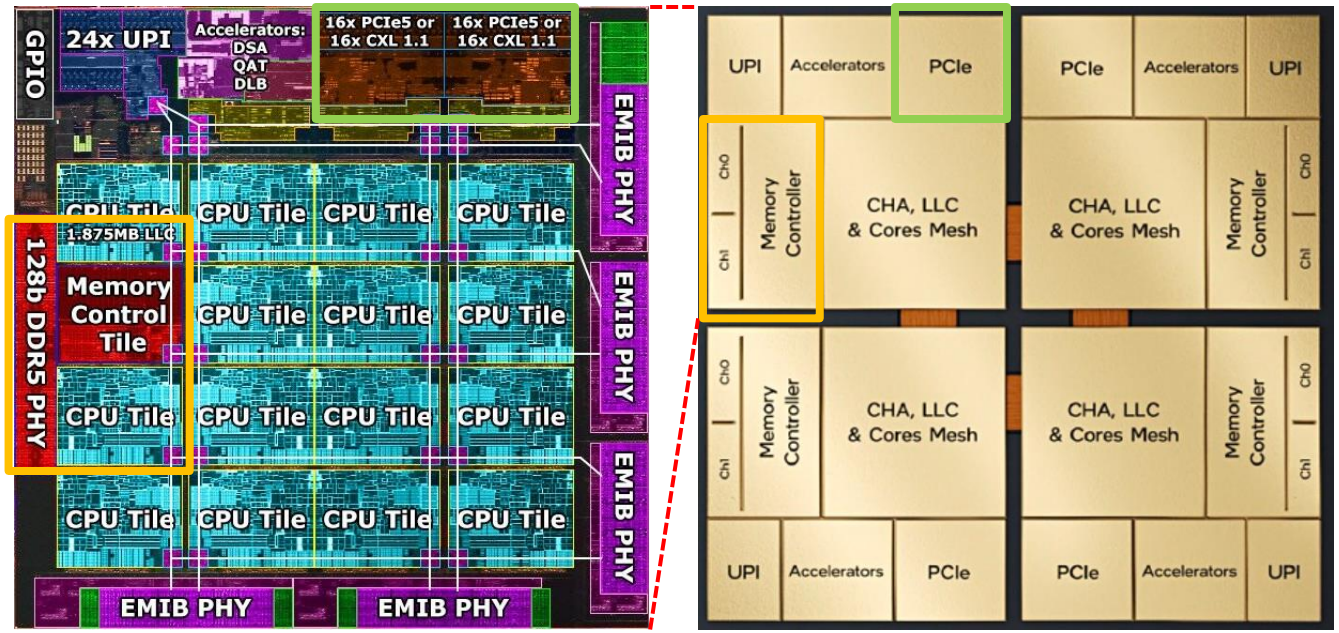

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ECO-CHIP framework

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  - Manufacturing
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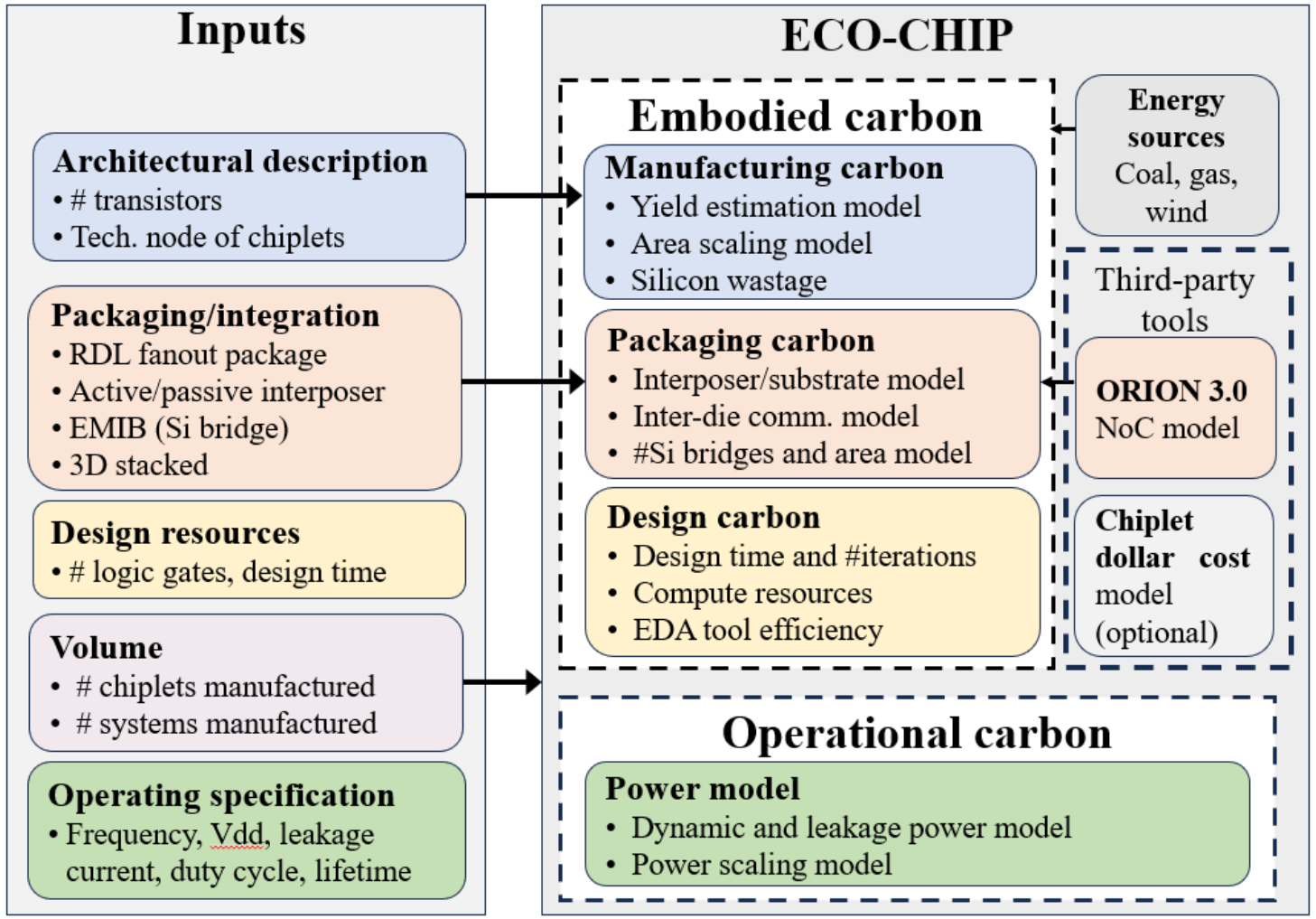
  - Design
- Operational CFP
- Integrate with third-party tools



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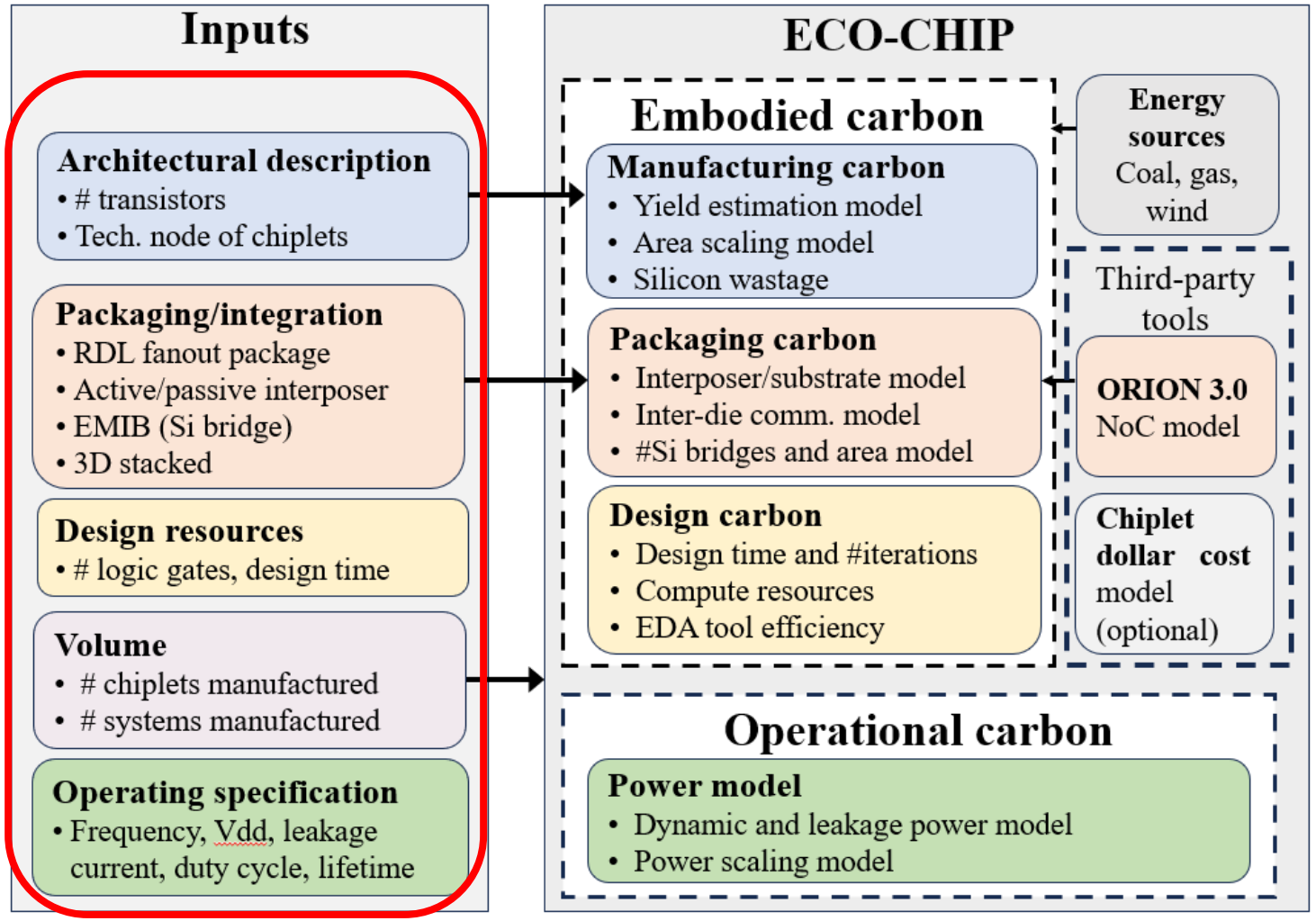

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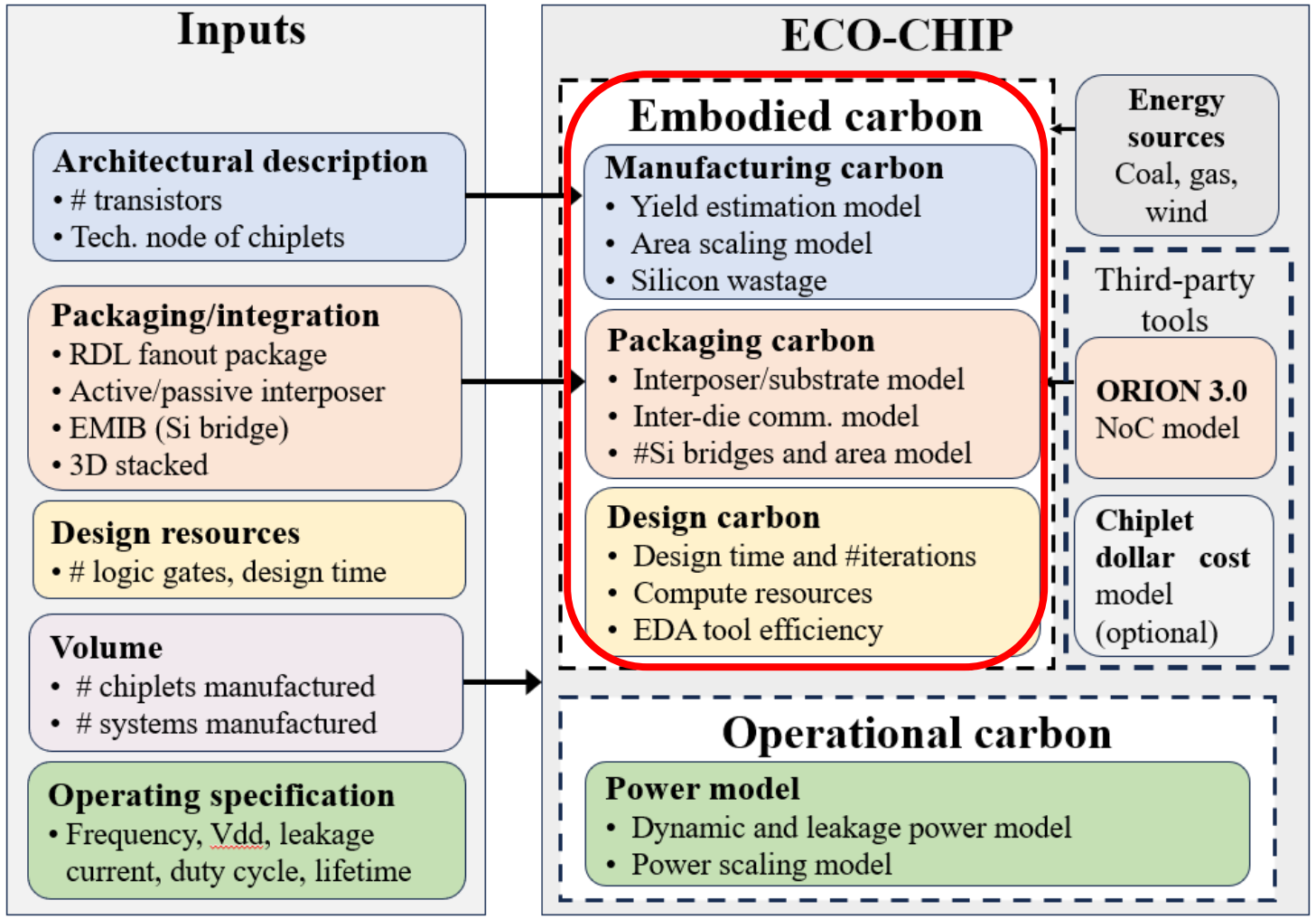

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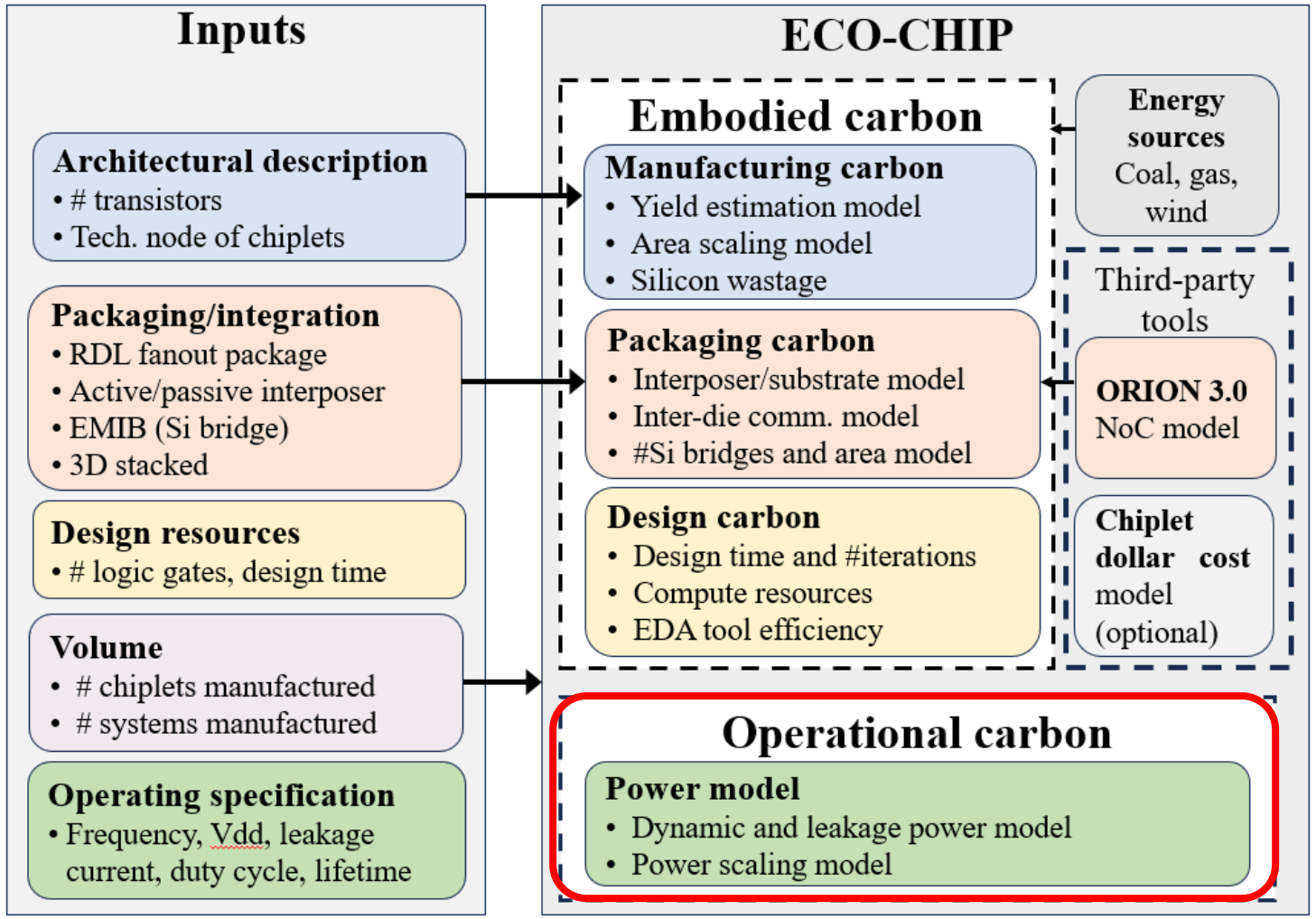

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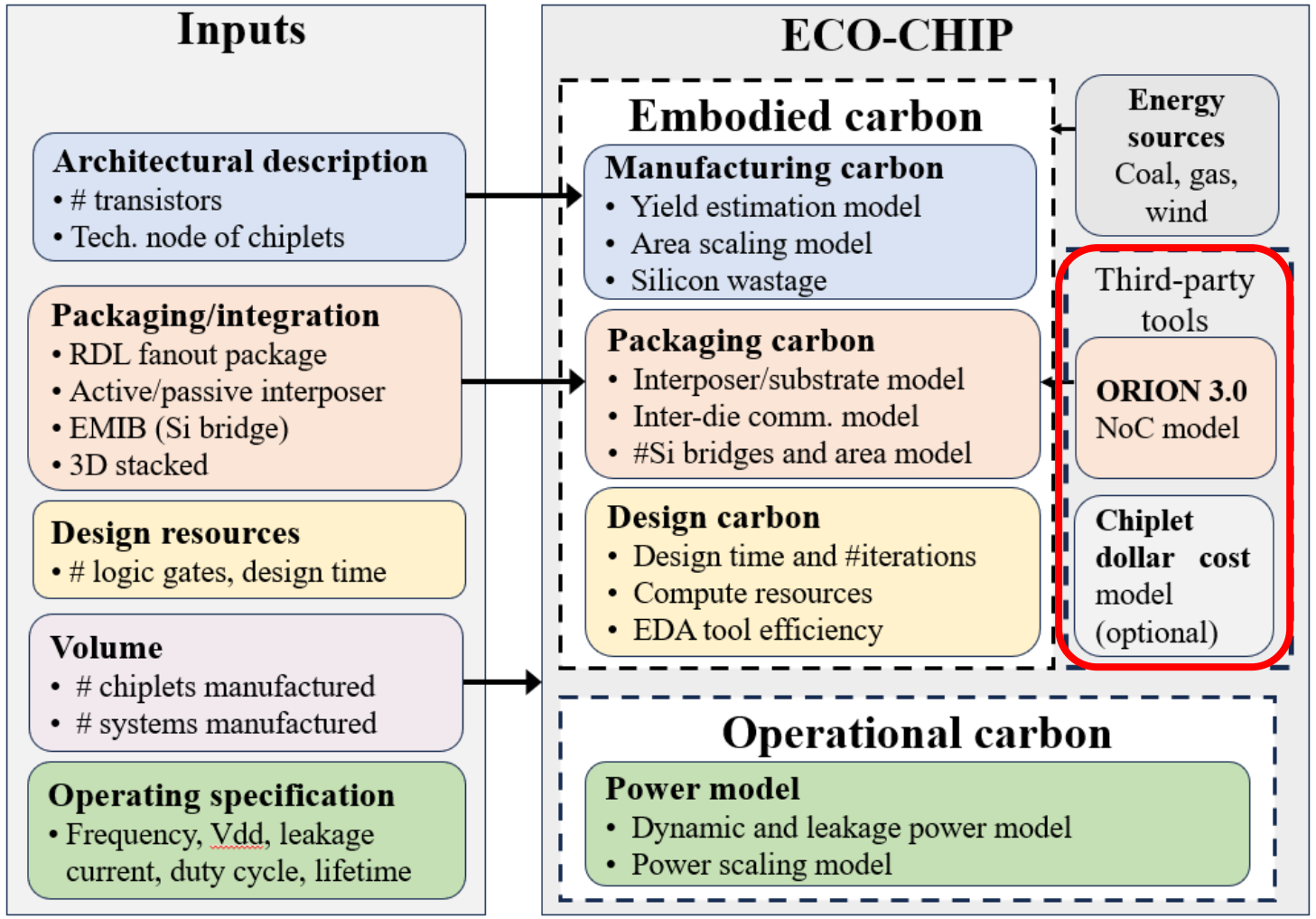


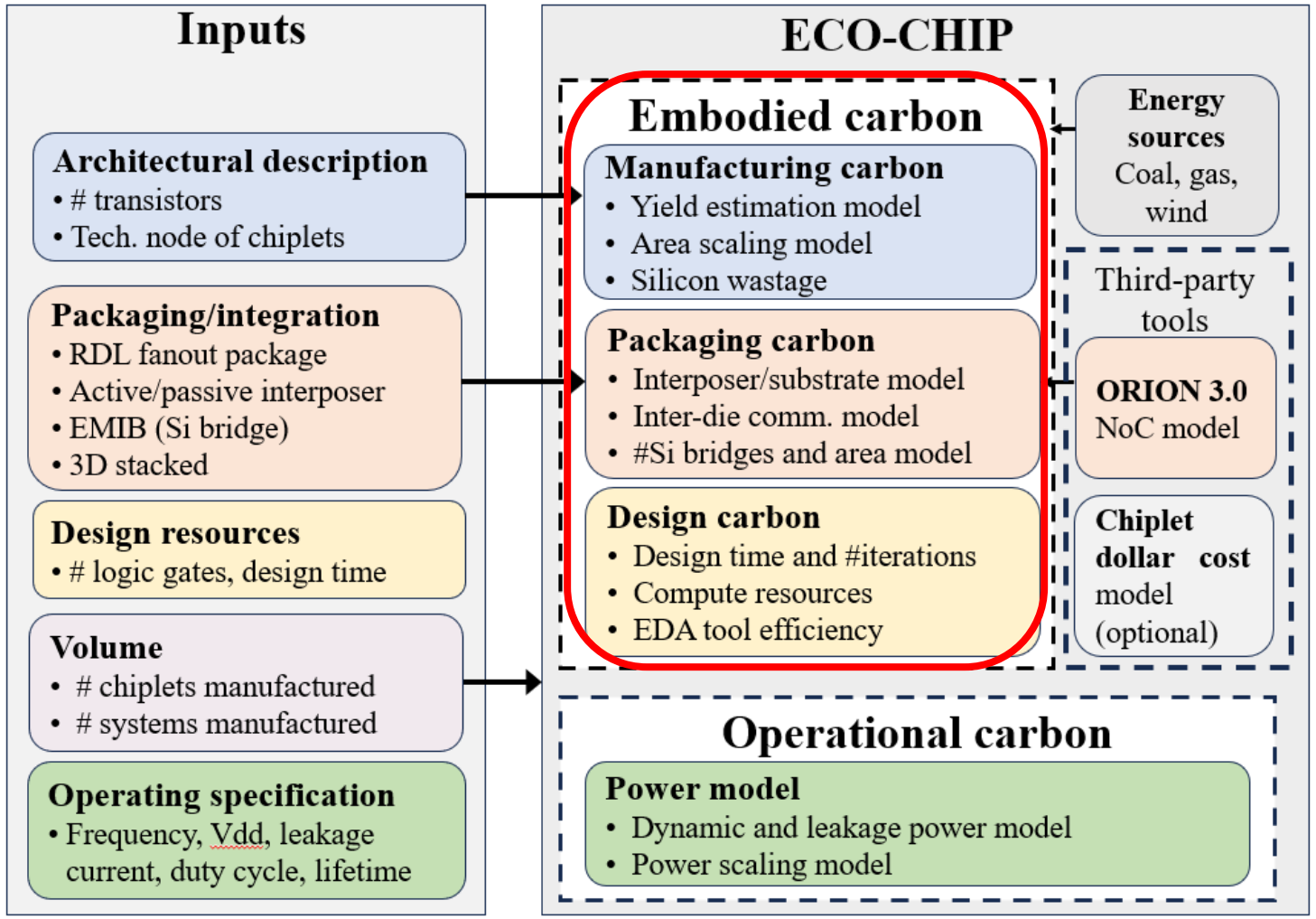
ECO-CHIP framework

Total carbon is given by the sum of operational carbon across the lifetime of the chip and the embodied carbon

$$C_{tot} = C_{emb} + lifetime \times C_{op}$$

$$C_{emb} = C_{mfg} + C_{HI} + C_{des}$$

C_{emb} - Embodied carbon
C_{mfg} - Manufacturing carbon
C_{des} - Design carbon
C_{HI} - Carbon from HI (advanced packaging and area overheads)



ECO-CHIP framework

Total carbon is given by the sum of operational carbon across the lifetime of the chip and the embodied carbon

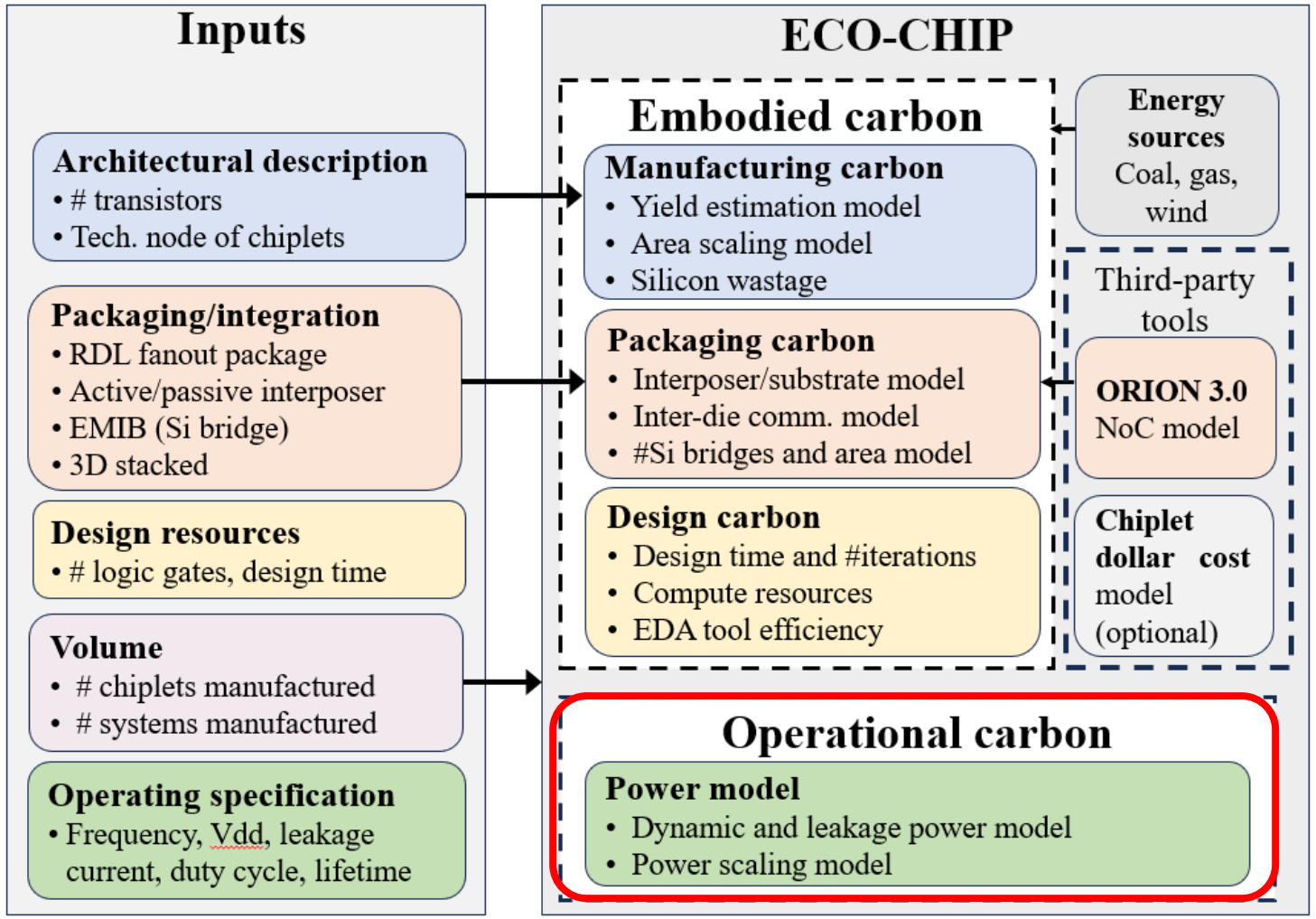
$$C_{tot} = C_{emb} + lifetime \times C_{op}$$

$$C_{op} = C_{src,use} \times E_{use}$$

C_{op} - Operational carbon

$C_{src,use}$-Carbon intensity of energy source

E_{use} - Energy spend during usage



Agenda

- Introduction
- Prior work
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- **ECO-CHIP**
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Embodied carbon: Manufacturing

The manufacturing carbon for a die depends on its area, and amortized wasted area on the wafer

Embodied carbon: Manufacturing

The manufacturing carbon for a die depends on its area, and amortized wasted area on the wafer

$$C_{mfg} = CFPA \times (Die\ area + Wasted\ area)$$

$$CFPA = \frac{(\eta_{fab} \times C_{mfg} \times E_{mfg} + C_{gas} + C_{material})}{Yield}$$

η_{fab} - Energy efficiency of lithography tools

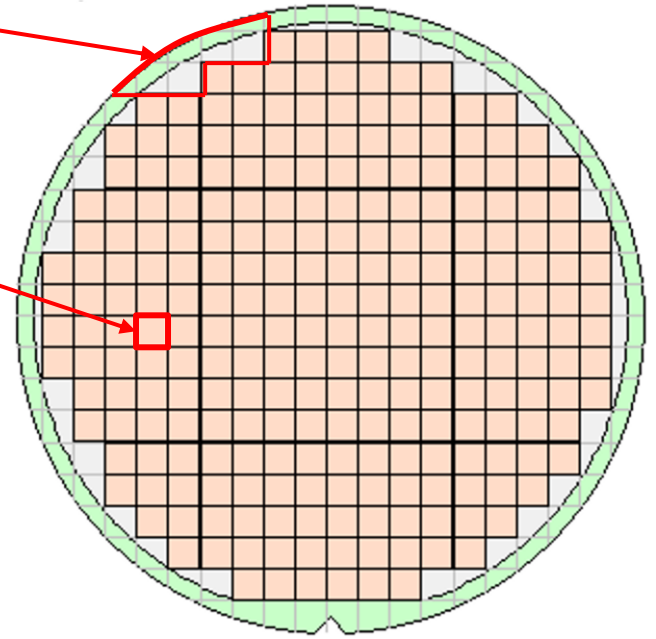
EPA - Energy consumed during manufacturing

C_{gas} - CFP from green house gas emission

$C_{material}$ - CFP from sourcing the materials for fabrication

$Yield$ - Yield of design for particular process node

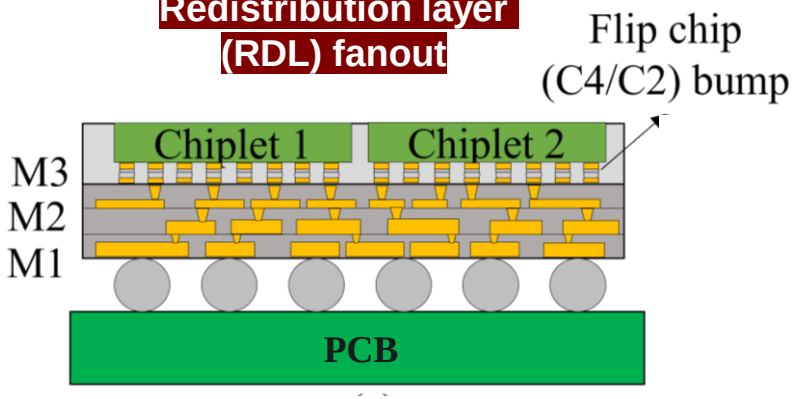
ACT (prior work)



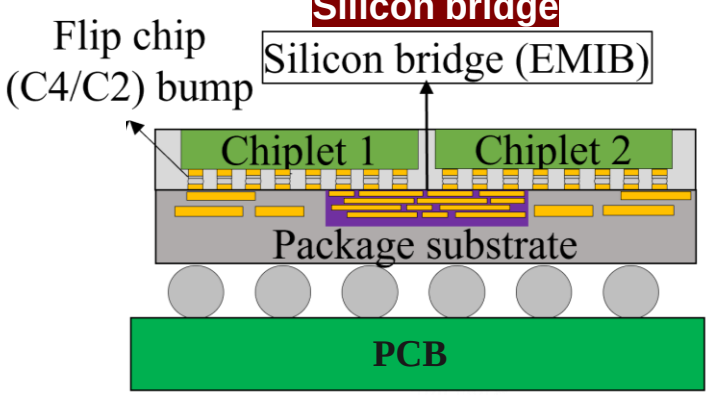
Enhanced the manufacturing carbon model from ACT to include area-dependent yield and efficiency of fabrication tools

Embodied carbon: HI overheads

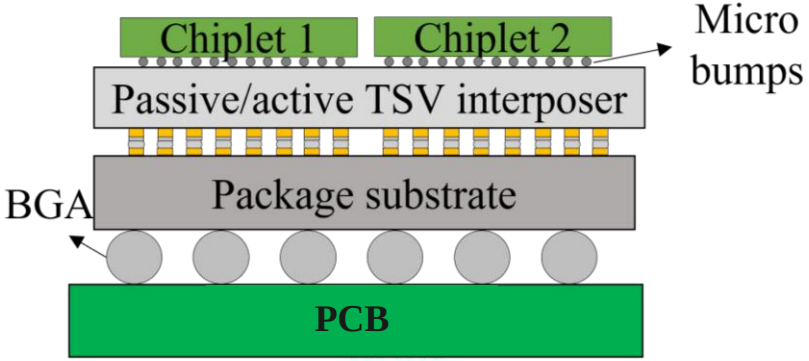
Redistribution layer (RDL) fanout



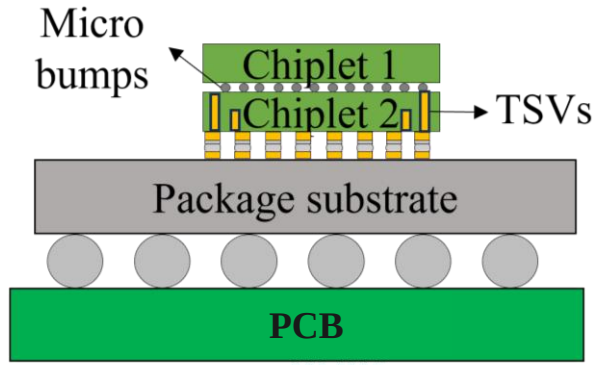
Silicon bridge



Passive/active interposer package



3D chiplet stacking



Embodied carbon: HI overheads

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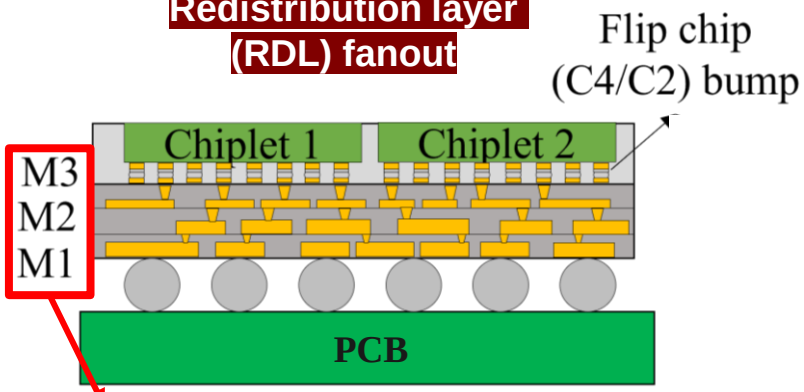
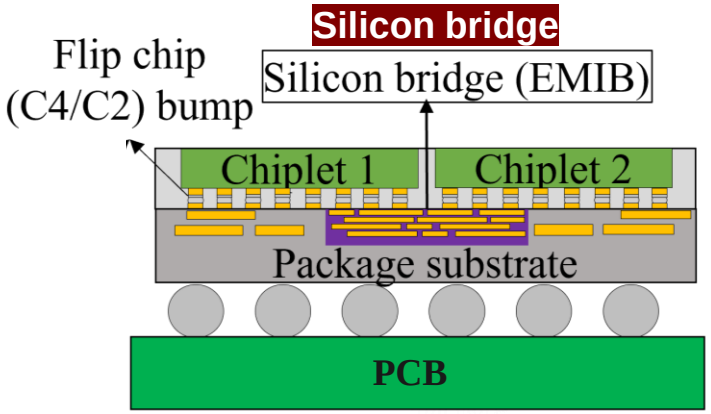


$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

Silicon bridge



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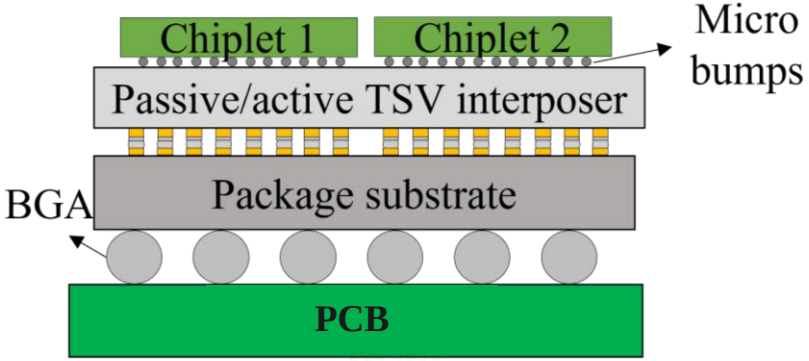
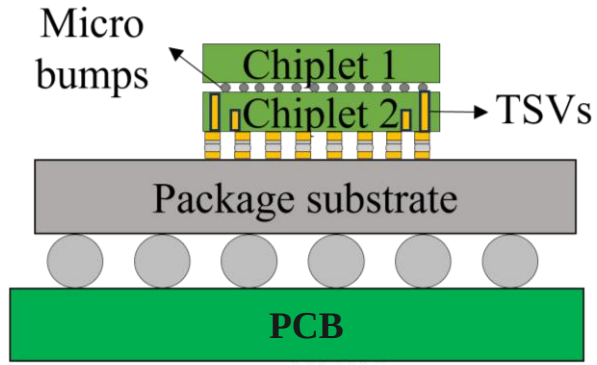


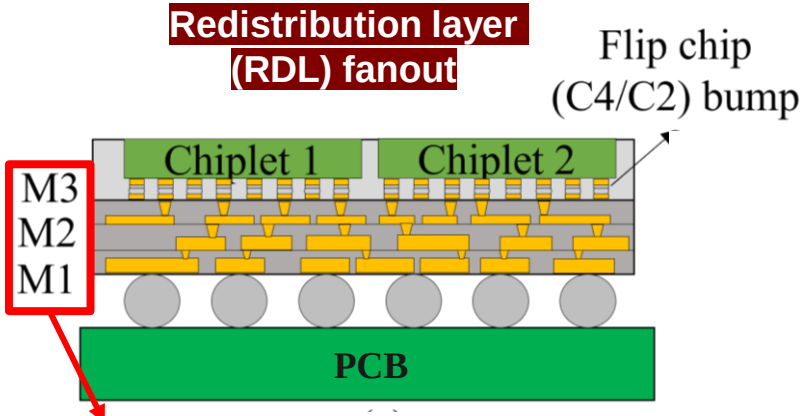
3D chiplet stacking



EPLA → Energy per unit area per layer

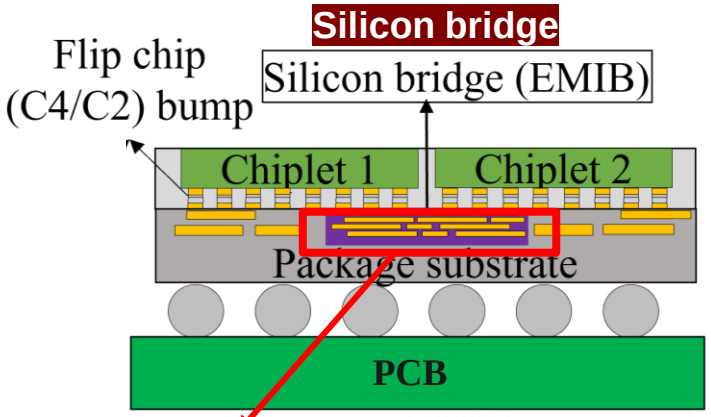
Embodied carbon: HI overheads

Redistribution layer (RDL) fanout



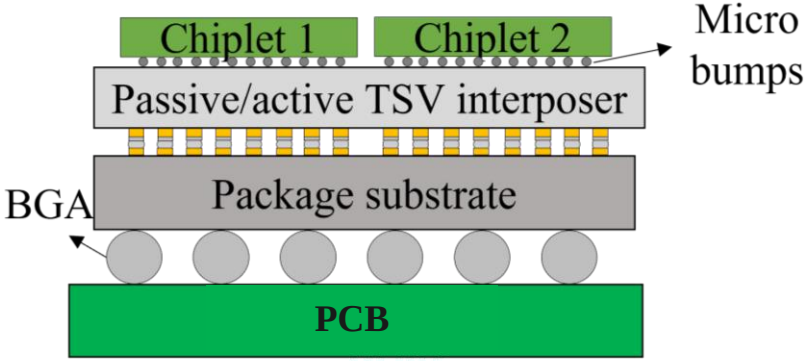
$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

Silicon bridge

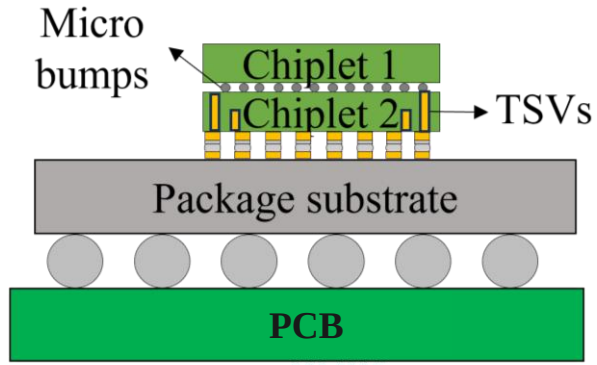


$$C_{bridge} = \frac{N_{bridge} \times L_{bridge} \times EPLA_{bridge} \times C_{pkg} \times A_{bridge}}{Yield(bridge)}$$

Passive/active interposer package



3D chiplet stacking



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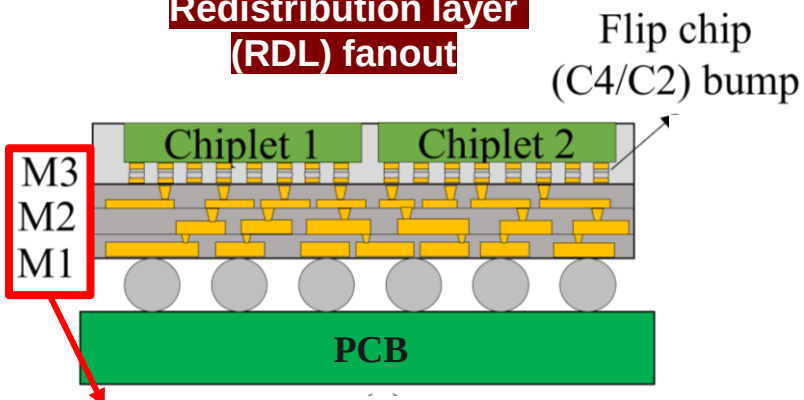
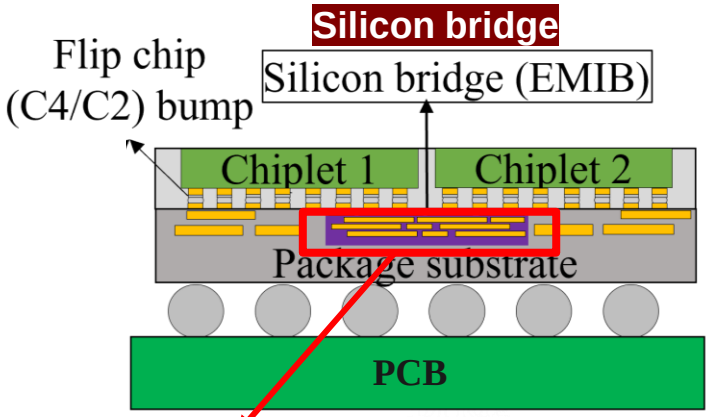


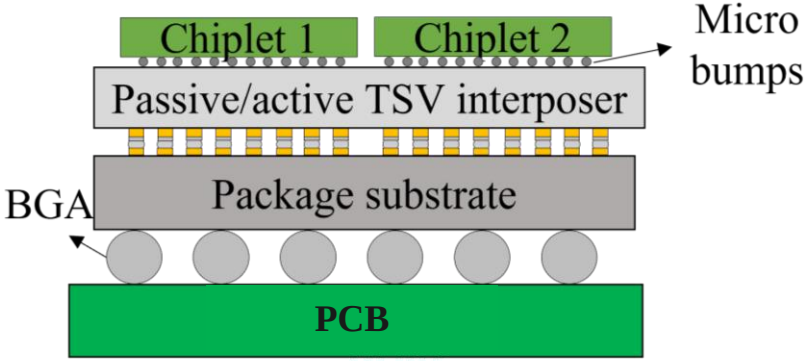
$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

Silicon bridge



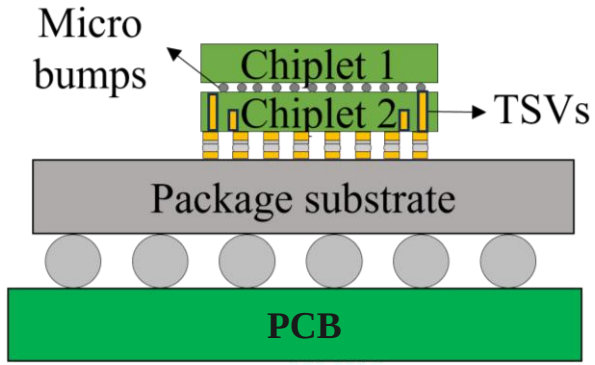
$$C_{bridge} = \frac{N_{bridge} \times L_{bridge} \times EPLA_{bridge} \times C_{pkg} \times A_{bridge}}{Yield(bridge)}$$

Passive/active interposer package



Modeled as an additional die

3D chiplet stacking



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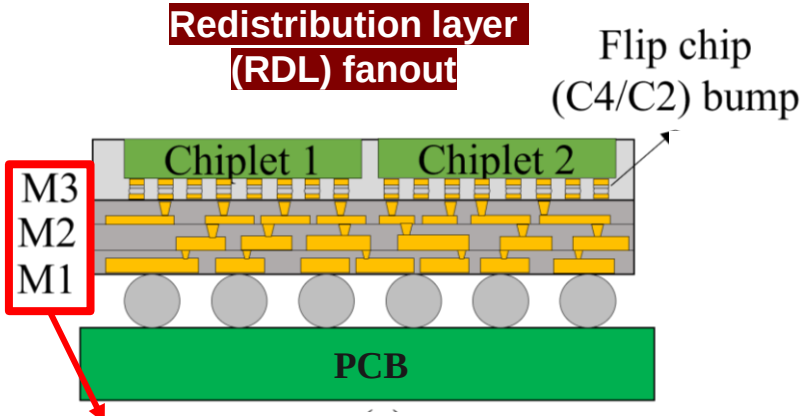
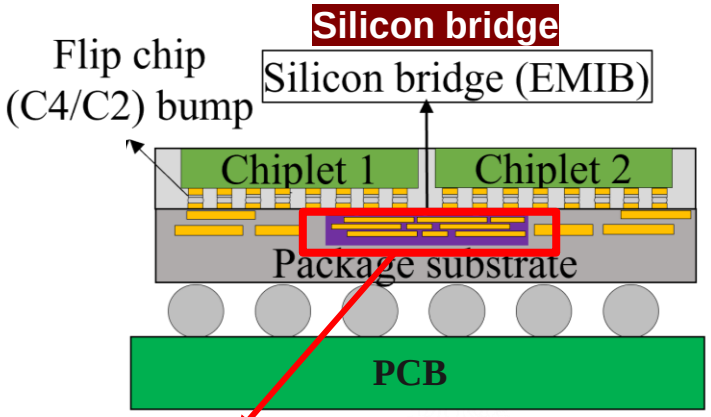


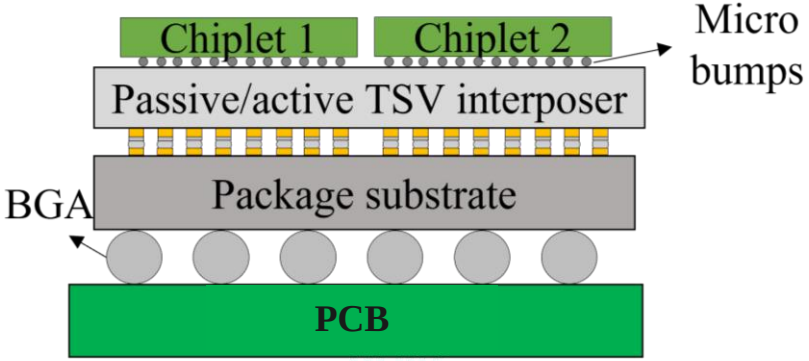
$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

Silicon bridge



$$C_{bridge} = \frac{N_{bridge} \times L_{bridge} \times EPLA_{bridge} \times C_{pkg} \times A_{bridge}}{Yield(bridge)}$$

Passive/active interposer package



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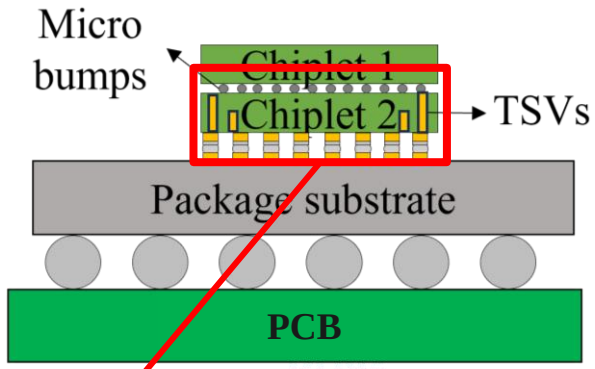
3D chiplet stacking



$$C_{3D} = \frac{N_{TSV,bump,bond} \times EPLA_{TSV,bump,bond} \times C_{pkg}}{Yield(3D)}$$

EPLA → Energy per unit area per layer

Embodied carbon: Design carbon

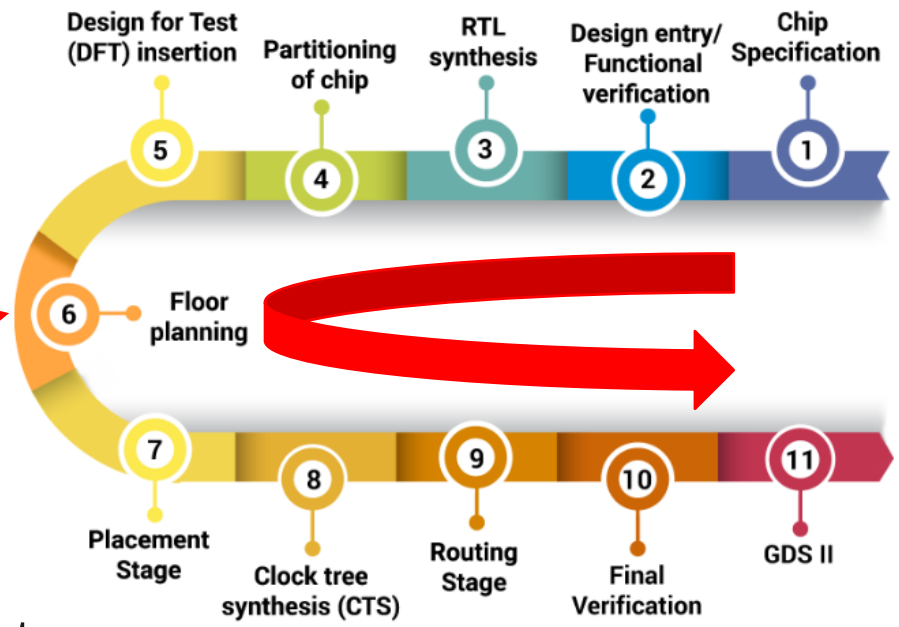
Design carbon of the system is the sum of:

- Design carbon of all chiplets amortized across the number of chiplets manufactured (design reuse)
- Design carbon of the overhead of integrating amortized across the number of systems packaged

The design carbon of a single chiplet is:

$$C_{des} = t_{des} \times P_{des} \times C_{src}$$

$$t_{des} = \frac{t_{verif} + (t_{SP\&R} + t_{analyze}) \times N_{des}}{\eta_{EDA}}$$



Source: eInfochips

$t_{verif,i}$ - Compute time for verification
$t_{SP\&R,i}$ - Computing time for single synthesis, place, and route
$t_{analyze,i}$ - Compute time for all simulation analysis
N_{des} - Number of design iterations
η_{EDA} - EDA tool productivity

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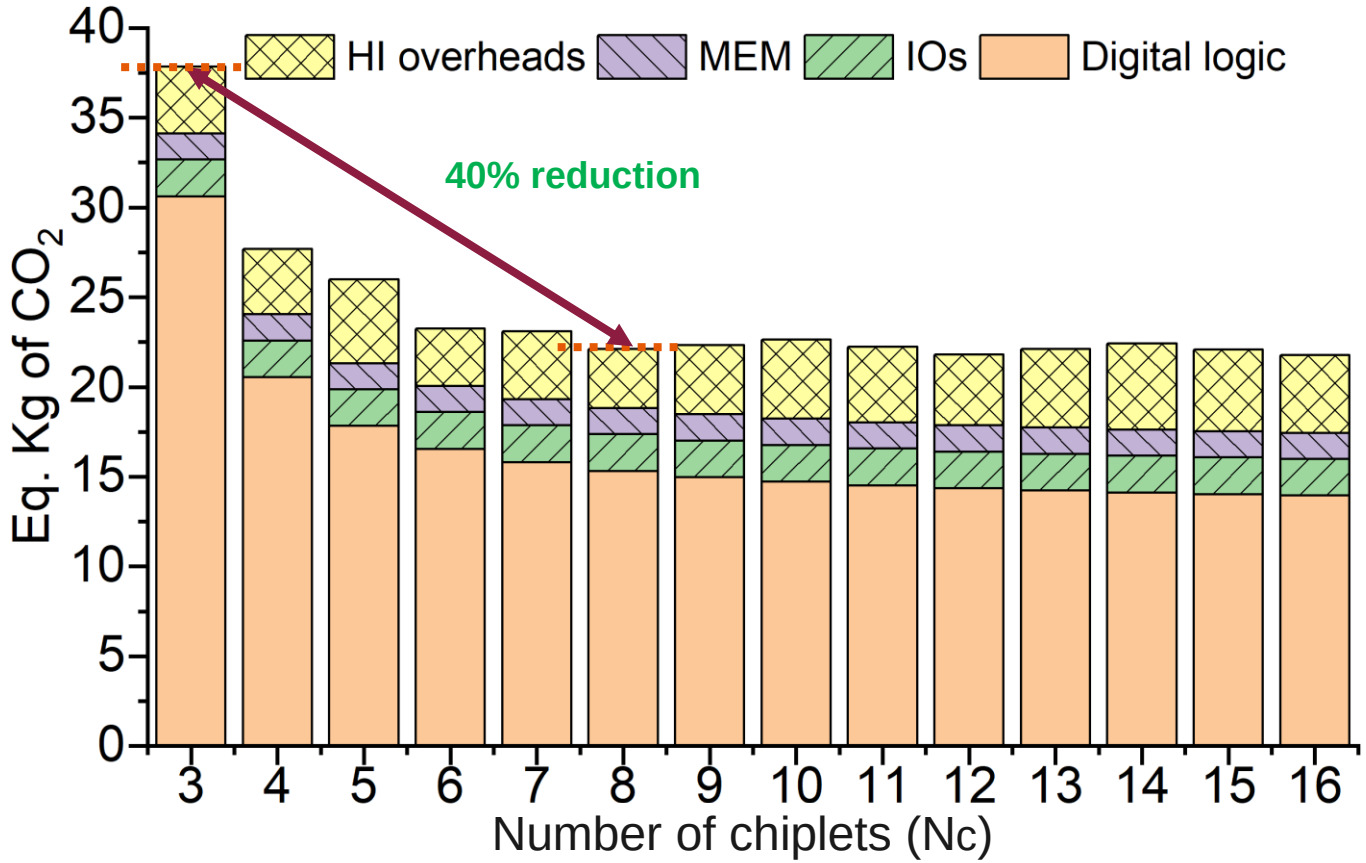
ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%

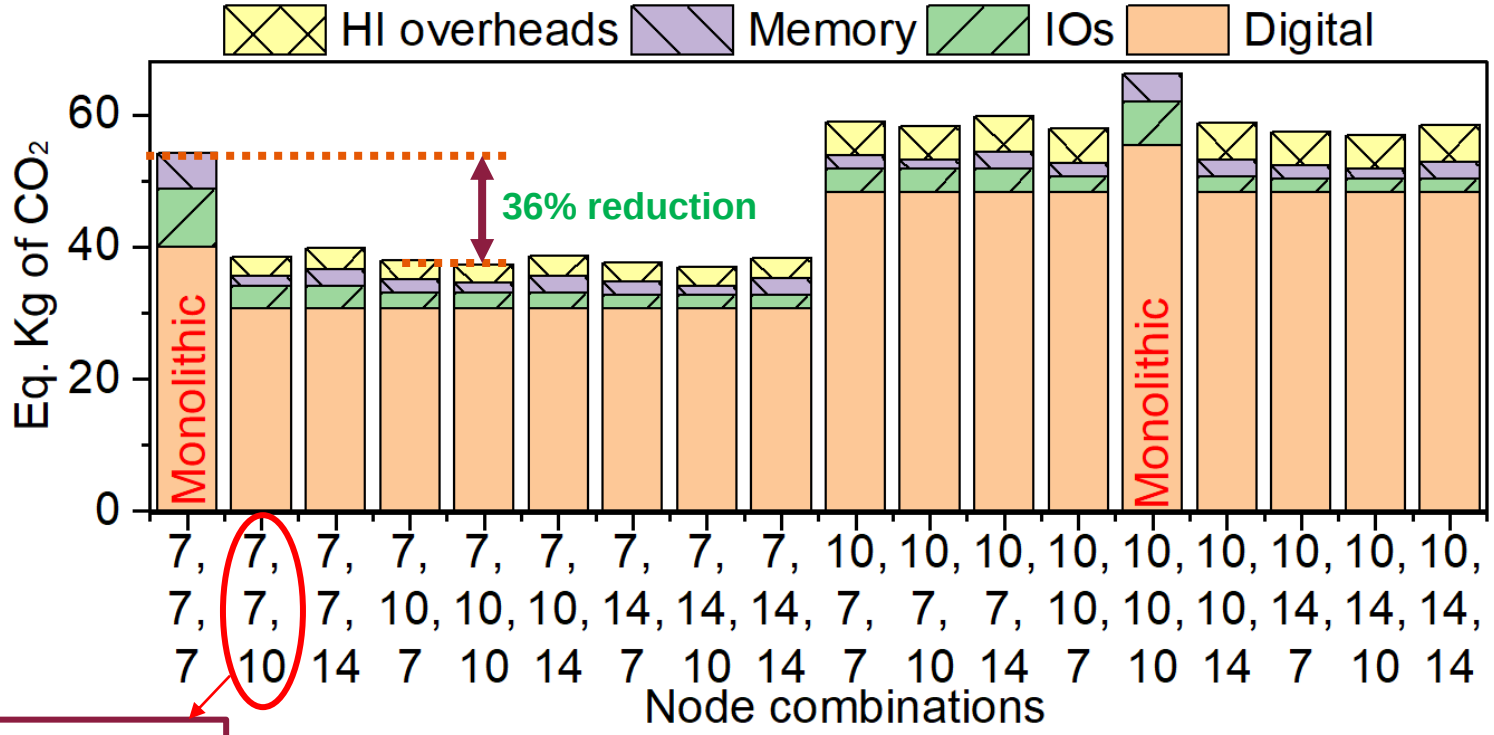
Sustainable Computing

Better yields with smaller chiplets



ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%
- Technology mix and match can help reduce overall CFP by 36%



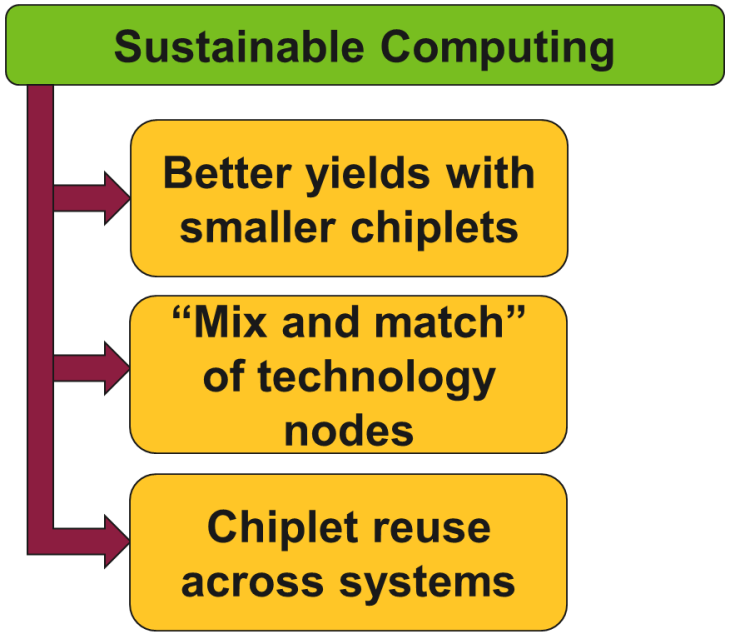
Sustainable Computing

- **Better yields with smaller chiplets**
- **"Mix and match" of technology nodes**

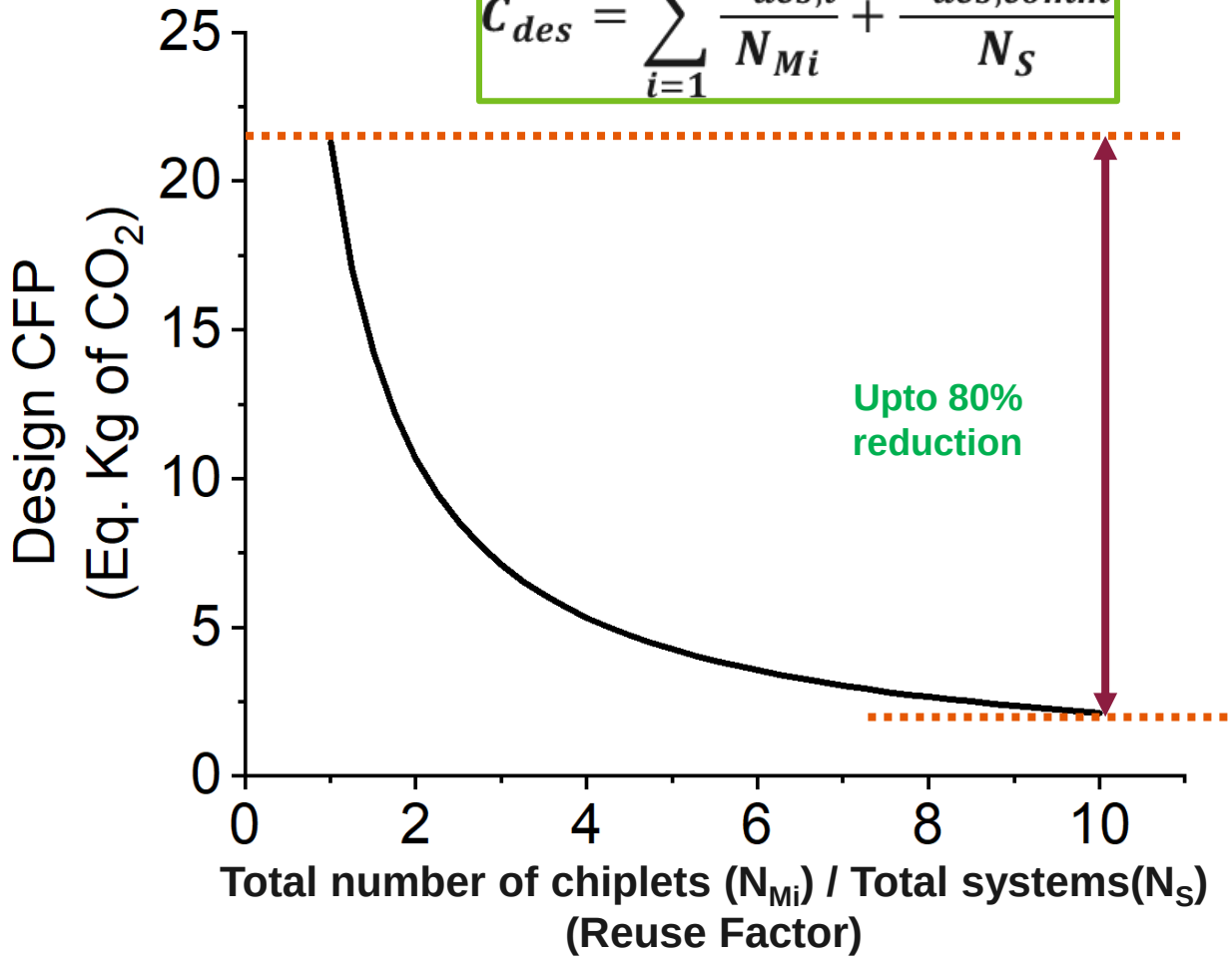
7,7,10 => 7nm Logic
7nm IOs
10nm Memory
7,7,7 => Monolithic on 7nm

ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%
- Technology mix and match can help reduce overall CFP by 36%
- Amortizing the design CFP across multiple systems can reduce design CFP by 80%

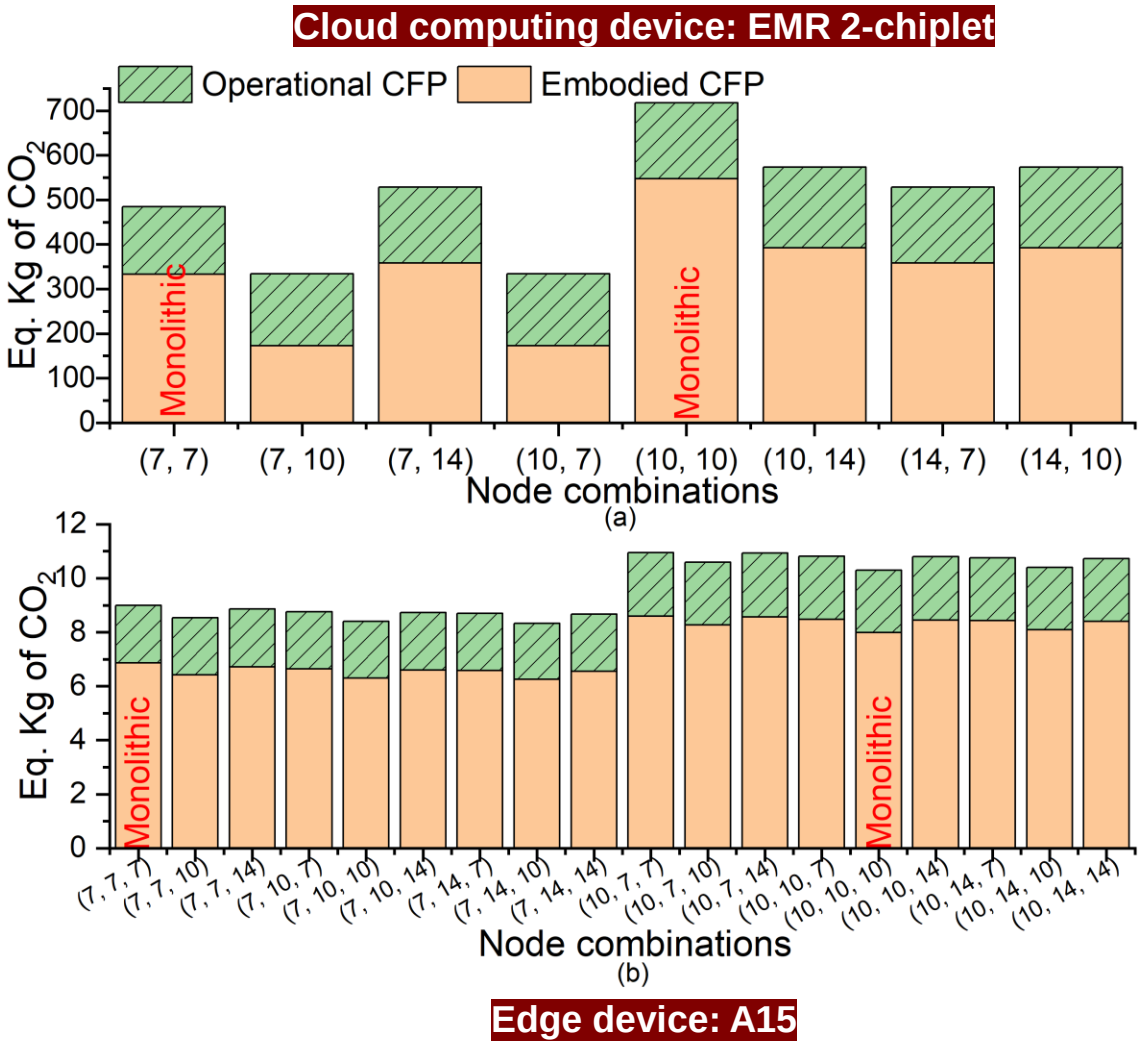


$$C_{des} = \sum_{i=1}^{Nc} \frac{C_{des,i}}{N_{Mi}} + \frac{C_{des,comm}}{N_S}$$



ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%
- Technology mix and match can help reduce overall CFP by 36%
- Amortizing the design CFP across multiple systems can reduce design CFP by 80%
- Edge devices
  - C_{emb} dominates, C_{op} already low
  - Disaggregation helps lower C_{emb}
- Cloud computing devices
  - Higher C_{op} / C_{emb} ratio
  - Disaggregation helps lower C_{emb}



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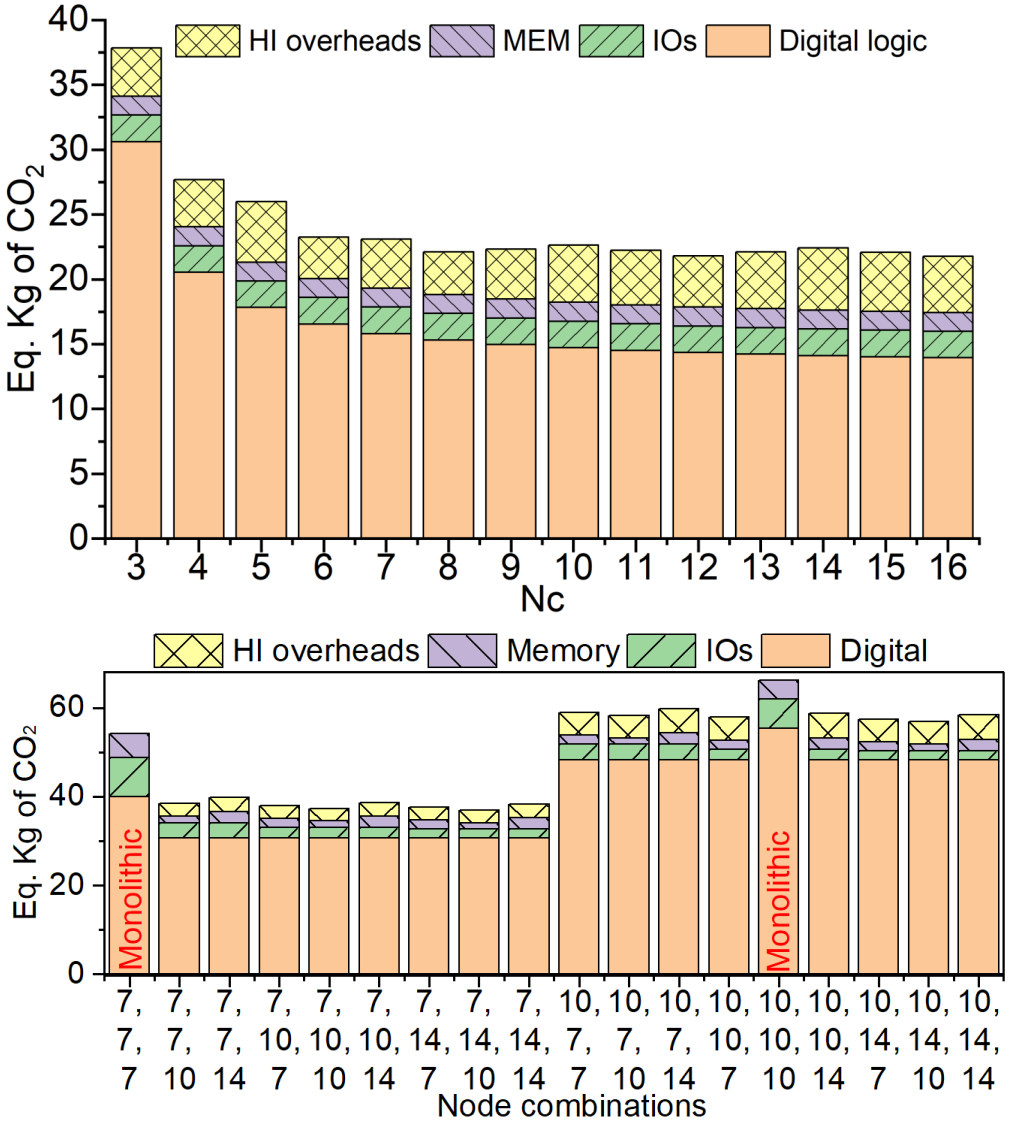
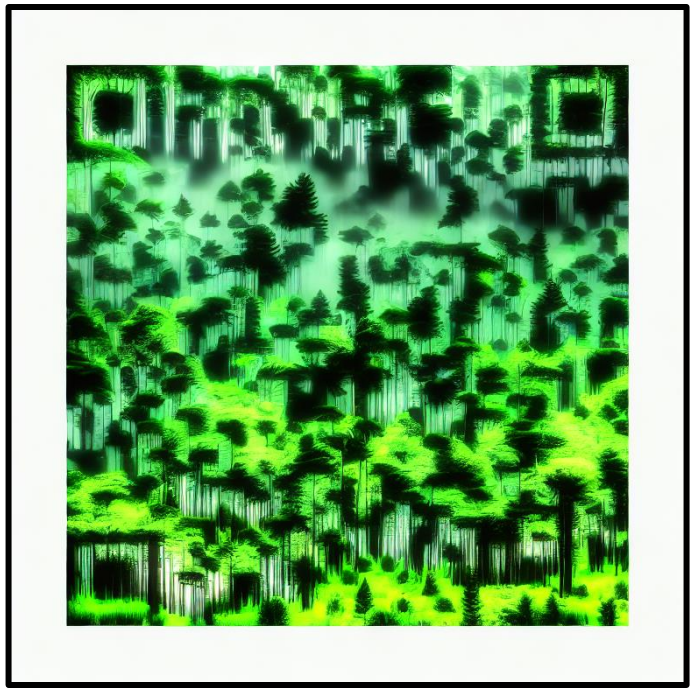
Conclusion

- Key contributions
  - Develop ECO-CHIP for heterogeneous systems
    - Model yield variations across multiple technology nodes for CFP analysis
    - CFP modeling for design
    - CFP of advanced packing architecture was modeled
  - HI systems are pathways to sustainable computing
    - Moving to chiplet-based design reduced CFP by **40%**
    - Can reduce up to **80%** of design CFP by amortizing and increasing the reuse factor
    - Chiplet and technology space exploration can reduce the overall CFP by **36%**



ECO-CHIP GitHub repository

- **We have open-sourced ECO-CHIP for broader access and awareness within the research community**



Scan QR code for ECO-CHIP

https://github.com/ASU-VDA-Lab/ECO-CHIP

README BSD-3-Clause license

ECO-CHIP : Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI

[paper]

Carbon footprint estimator for heterogenous chiplet-based systems. ECO-CHIP is an analysis tool that analyzes the operational and embodied CFP (design, manufacturing, and packaging). The tool supports the following HI and packaging architectures: RDL fanout, silicon bridge-based, passive and active interposer, and 3D integration. The tool evaluates the crucial package/assembly carbon emissions essential for HI systems, considering size, yield, and assembly process. In addition, it also estimates design CFP.

No packages published
Publish your first package

Contributors 2

VidyaChhabria

ChetanSudarshan Chetan Sudarshan

Languages

Python 100.0%

Suggested workflows

Published November 10, 2023 | Version v2

Software Open

ECO-CHIP: Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI: HPCA 2024 Artifact Evaluation

Choppali Sudarshan, Chetan[1]; Matkar, Nikhil[1]; Vrudhula, Sarma[1]; Sapatnekar, Sachin[2]; Chhabria, Vidya[1]

Hide affiliations

1. ROR Arizona State University
2. ROR University of Minnesota

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10.5281/zenodo.10223759

Thank you!!