# GreenFPGA: Evaluating FPGAs as Environmentally Sustainable Computing Solutions

Chetan Choppali Sudarshan, Aman Arora, Vidya A. Chhabria

DAC 2024

# Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- GreenFPGA
  - FPGA as sustainable computing solution
  - GreenFPGA framework
  - GreenFPGA modeling
- Results and analysis
- Conclusion and takeaway

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# Information and Computing Technology (ICT)

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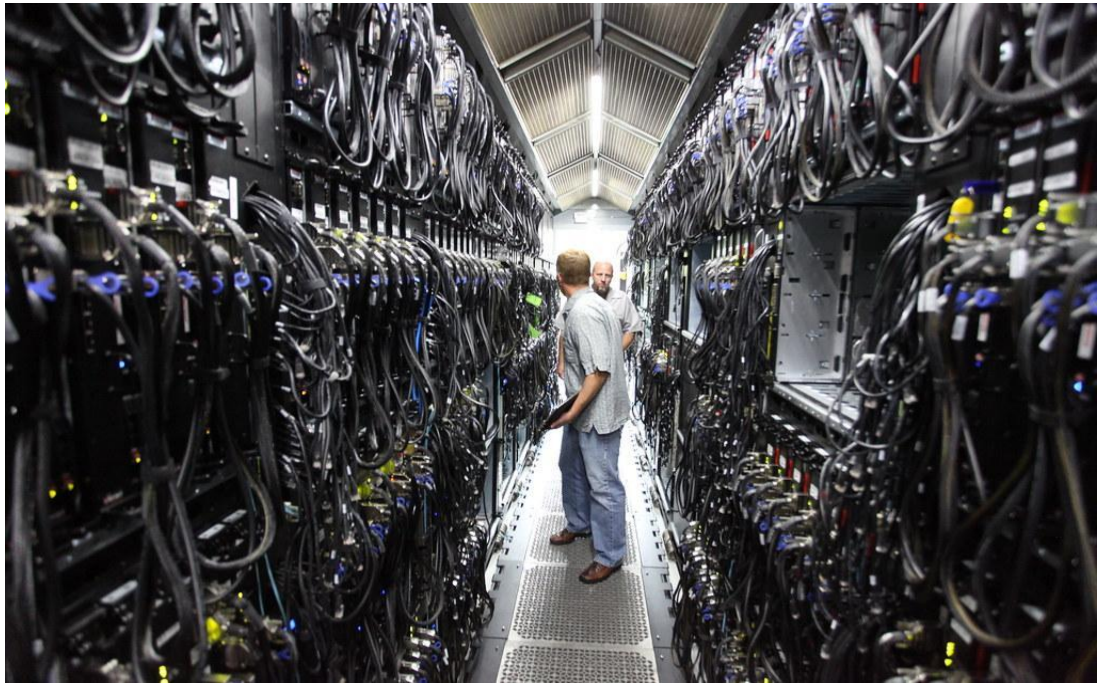

**User devices**

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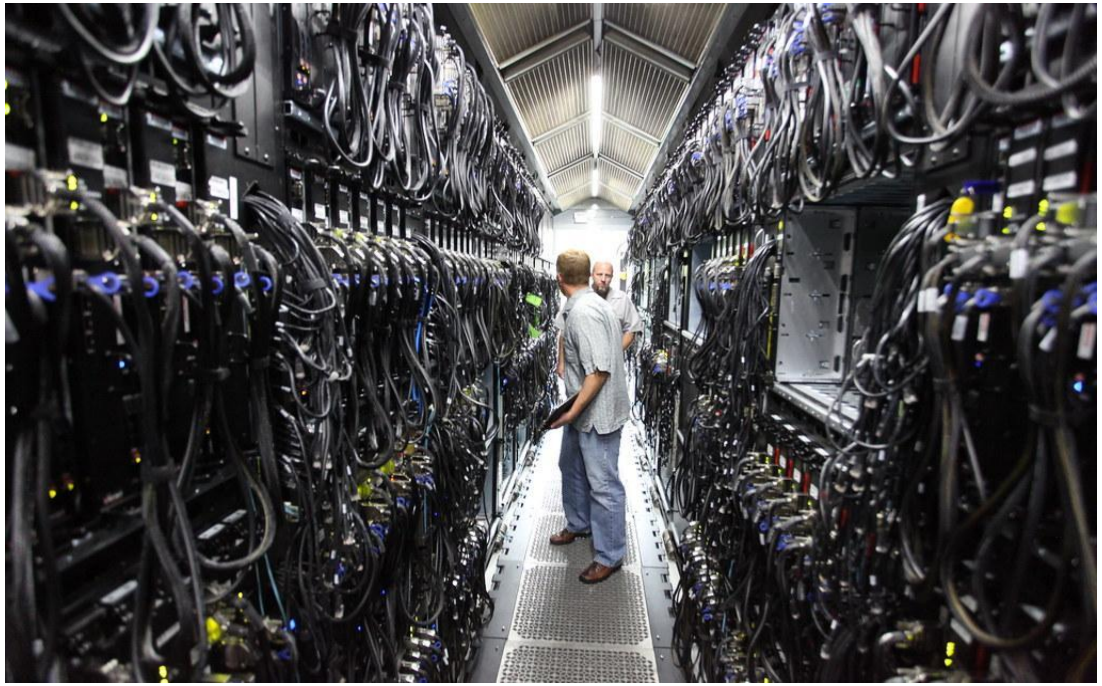


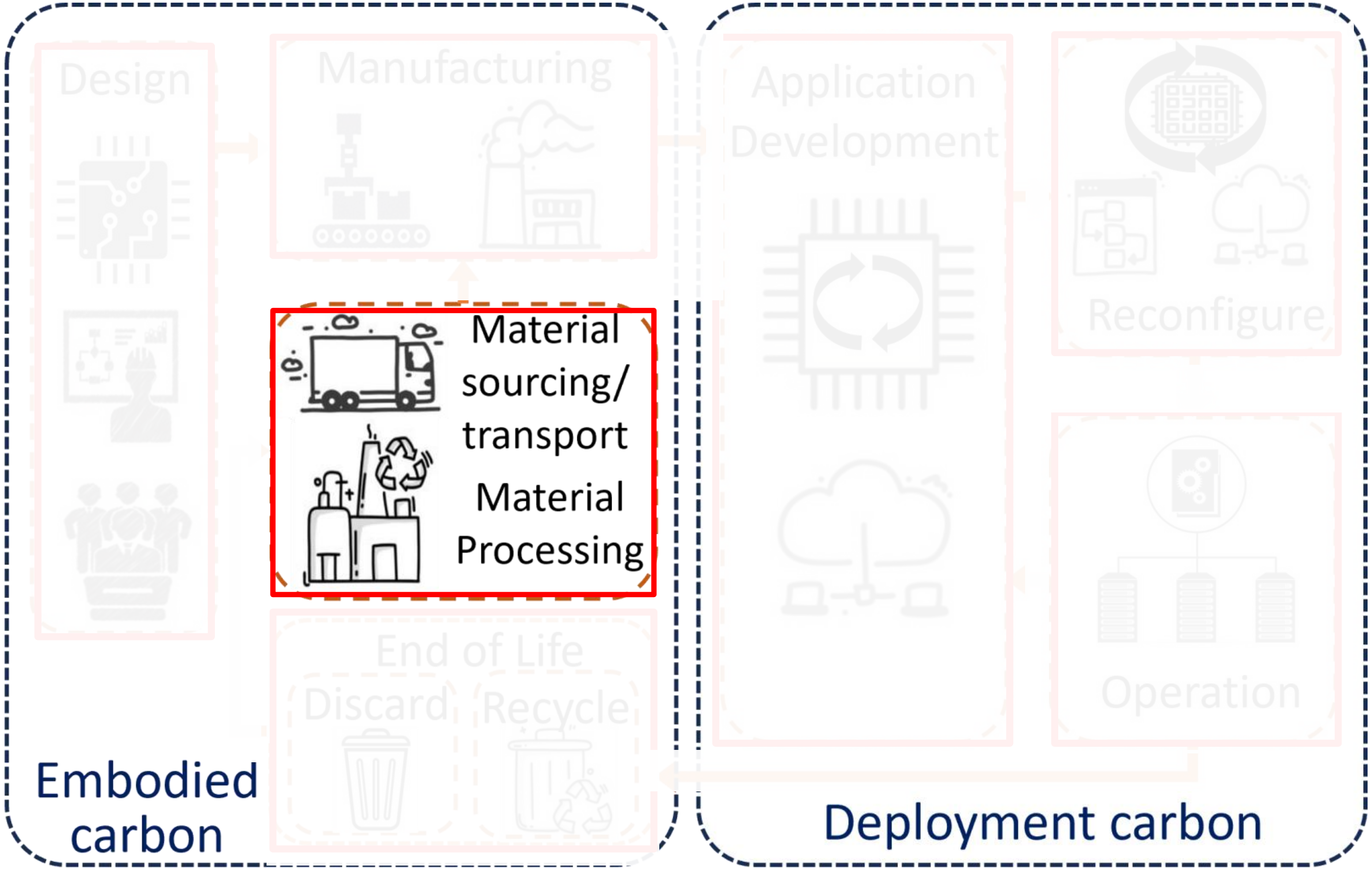
**User devices**


- ICT contributes to 3-4% of the total world CFP
- Need for sector-wide regulations

Source : C. Freitag et al., Patterns 2021

# Silicon lifecycle and sources of carbon

- **Embodied carbon footprint (CFP)**
  - Raw material CFP
  - Design CFP
  - Manufacturing and packing CFP
  - Deployment CFP
  - End of life CFP
- **Operational CFP**
  - CFP from end-user



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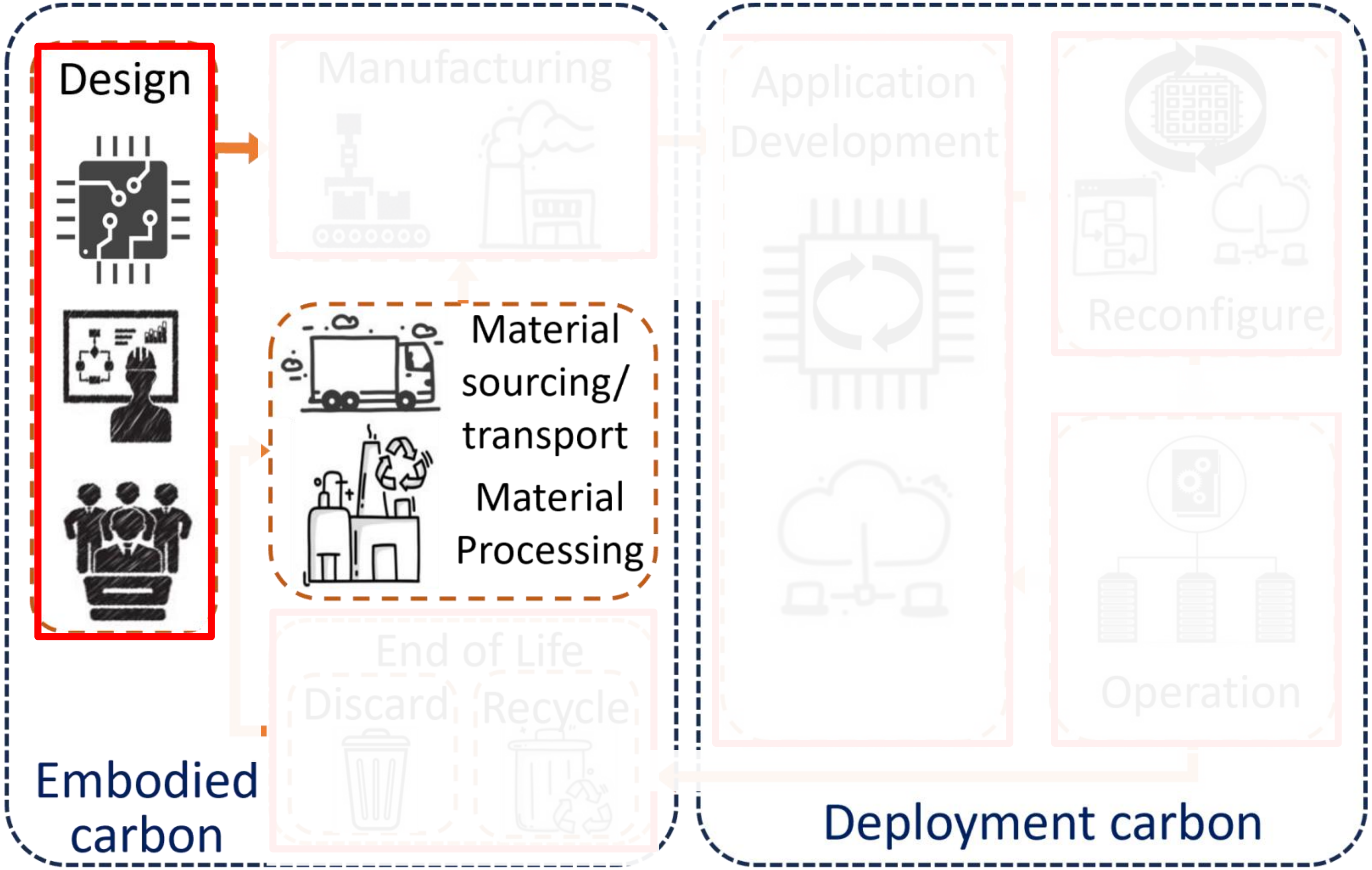

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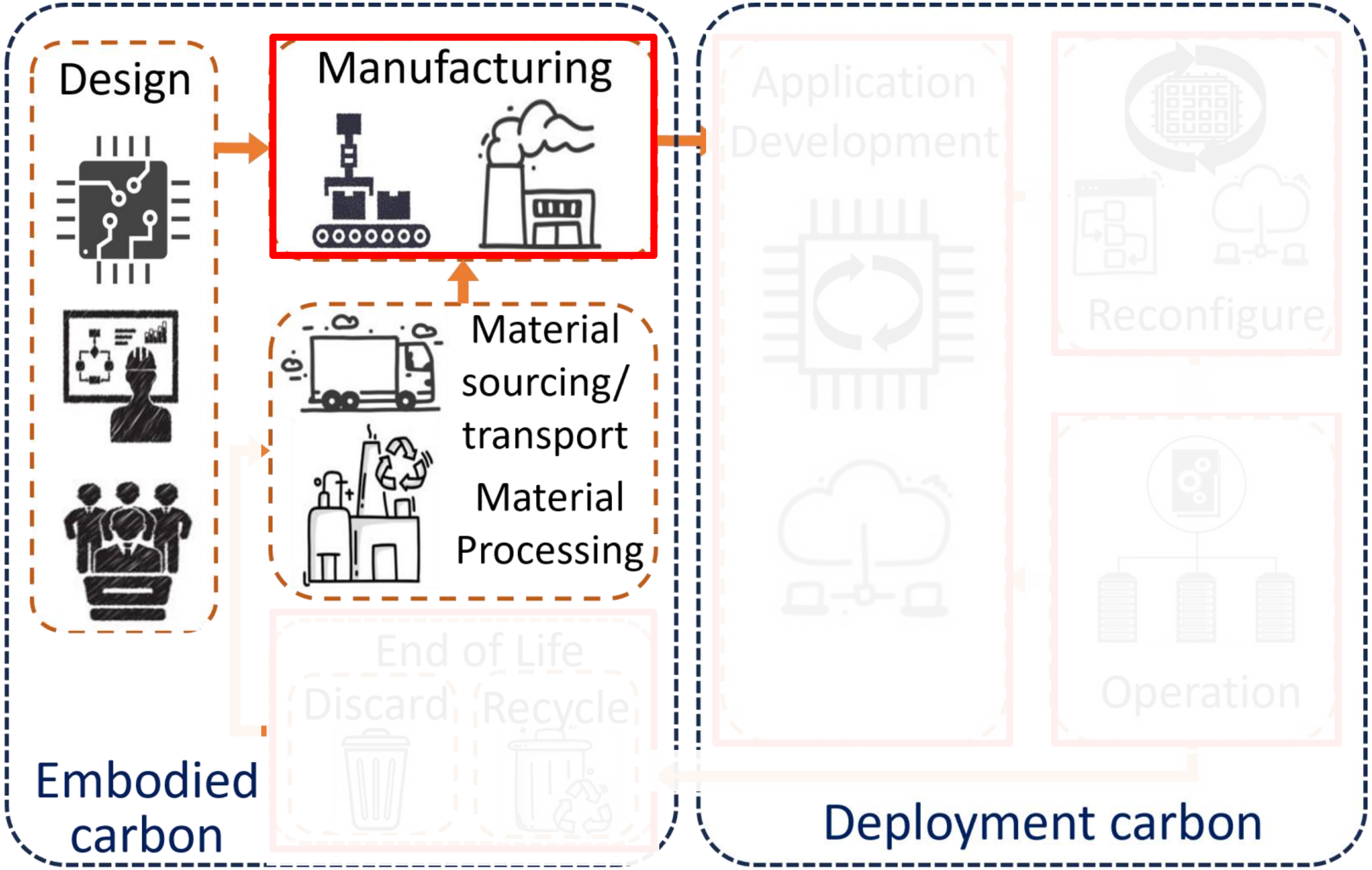

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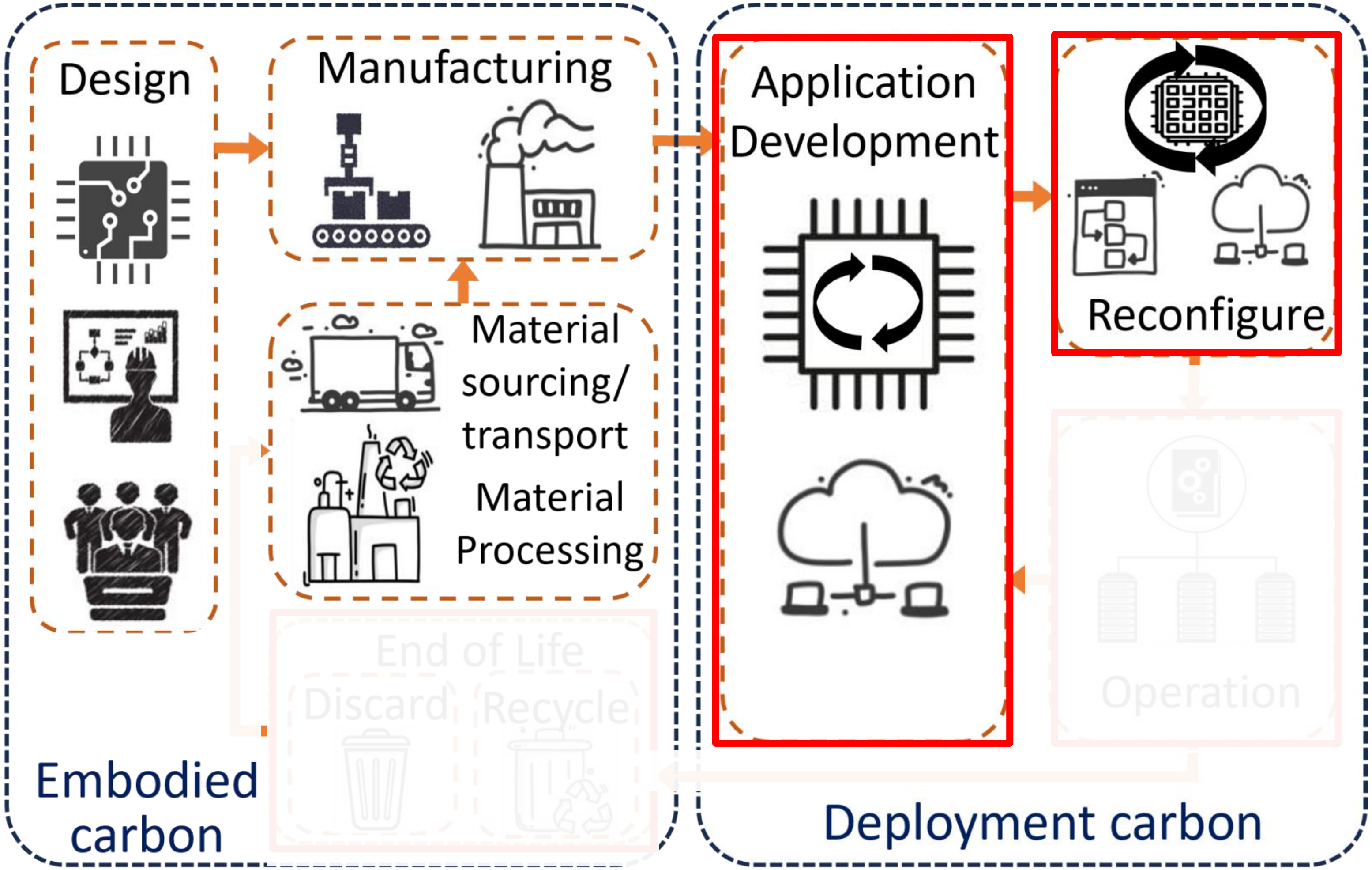

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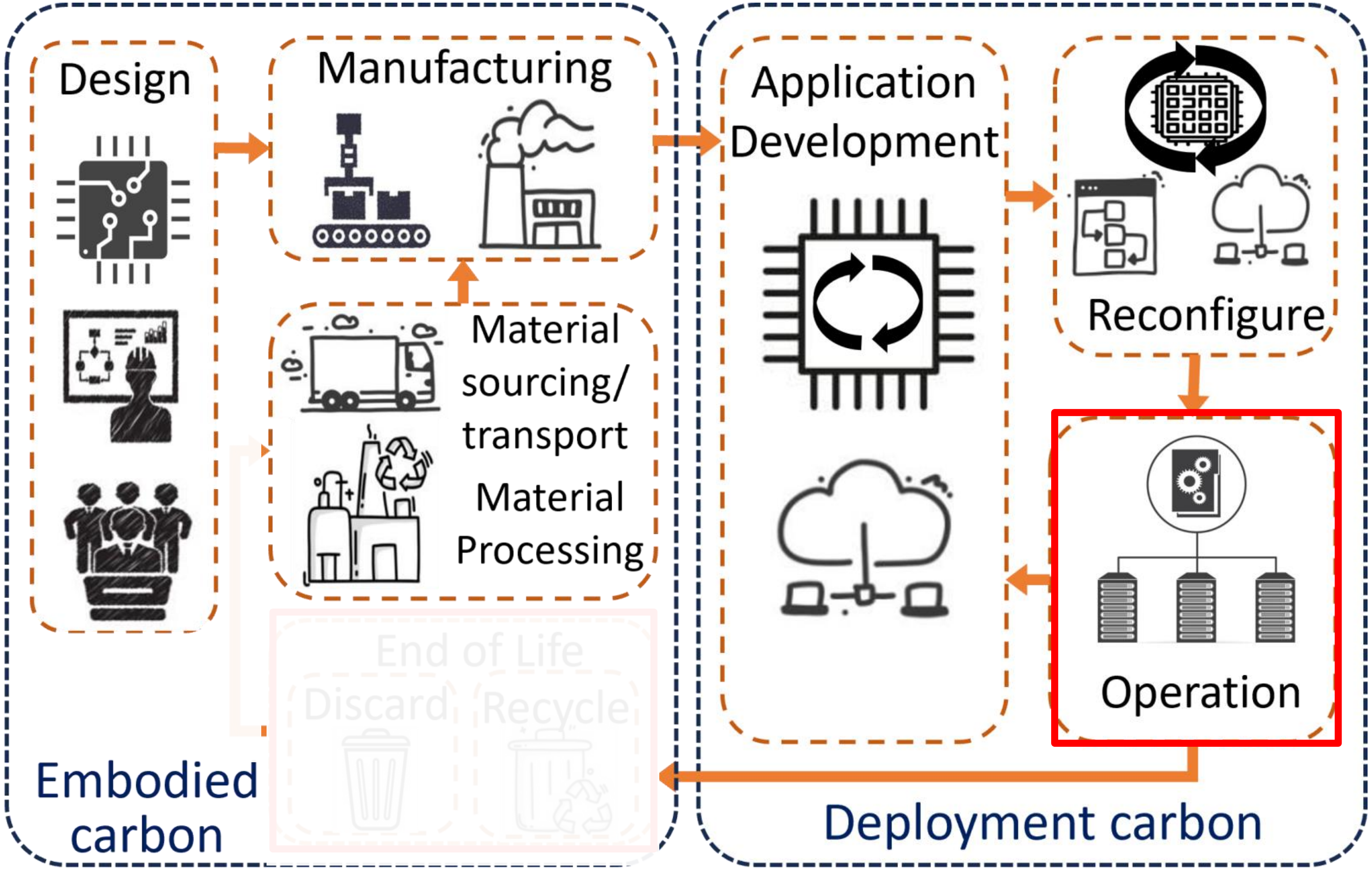

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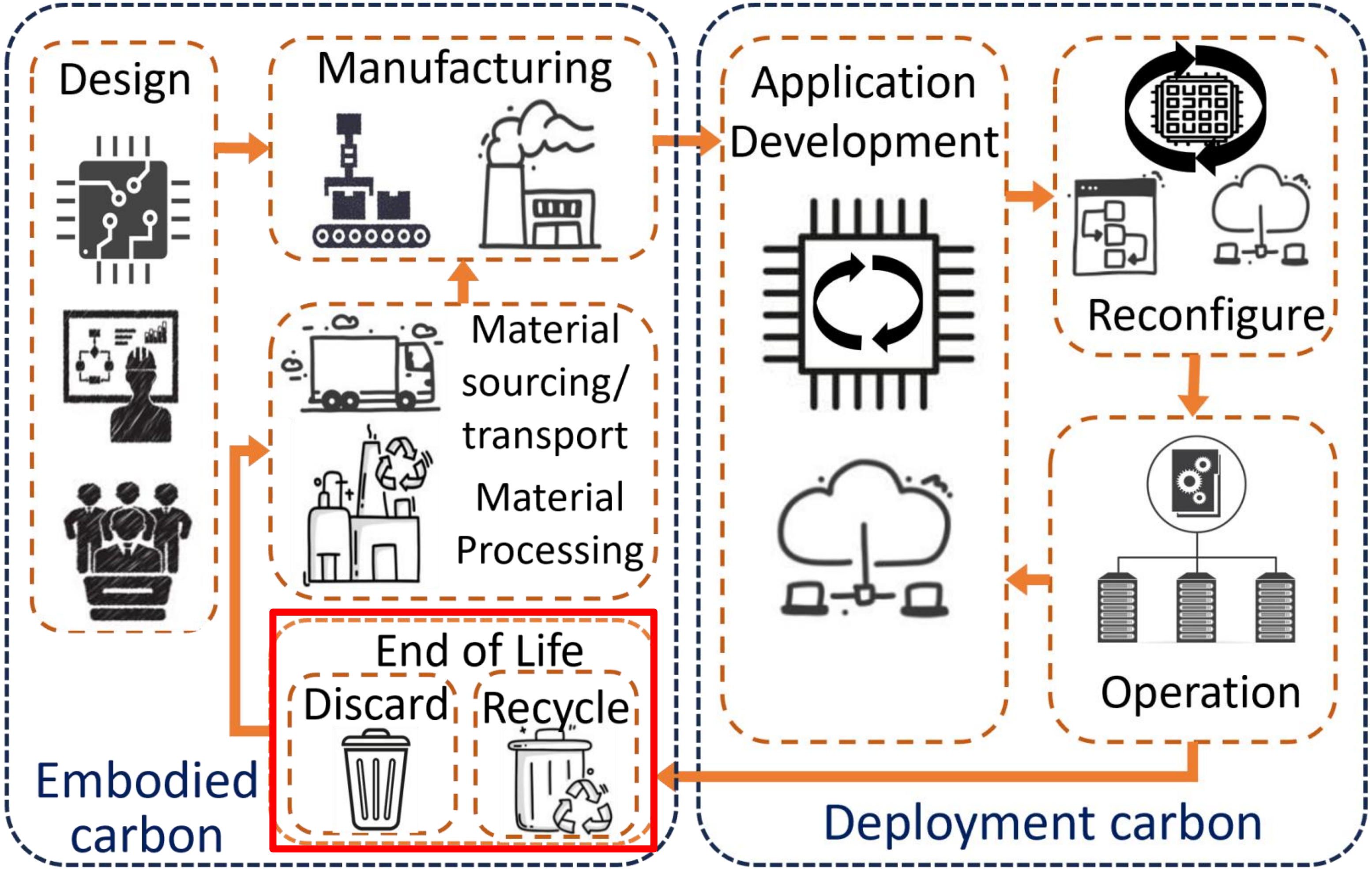

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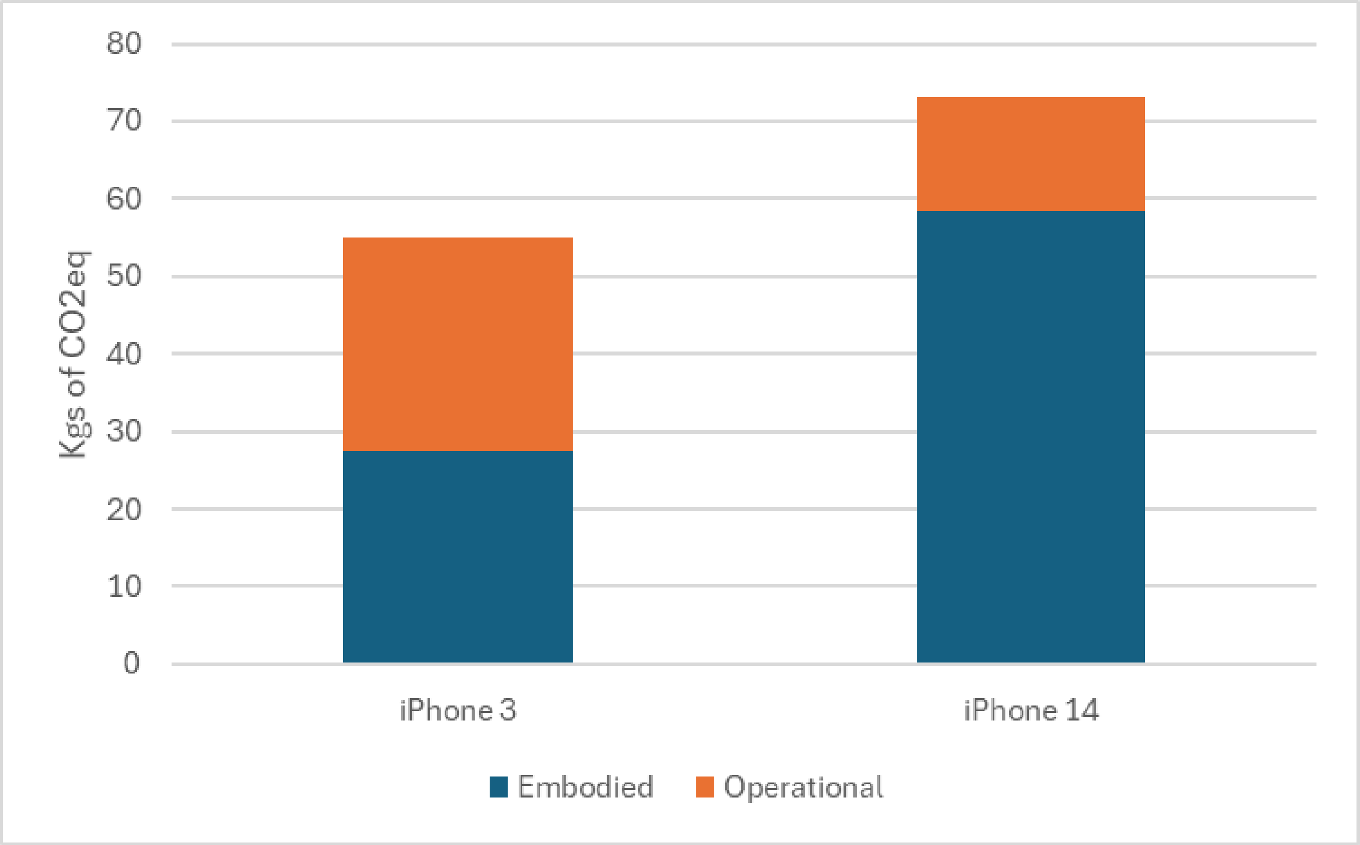


Source : Apple sustainability reports

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- Rising embodied carbon
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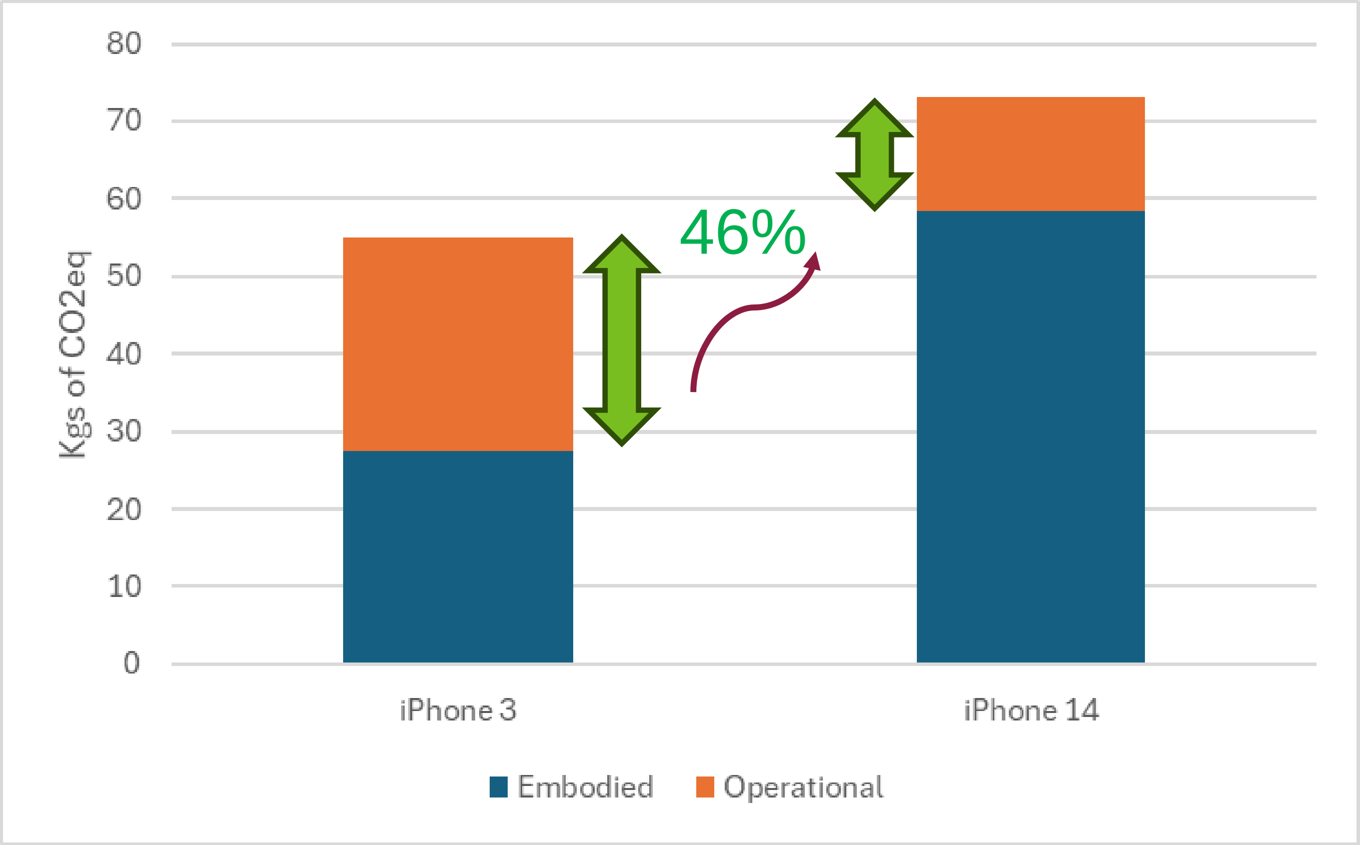


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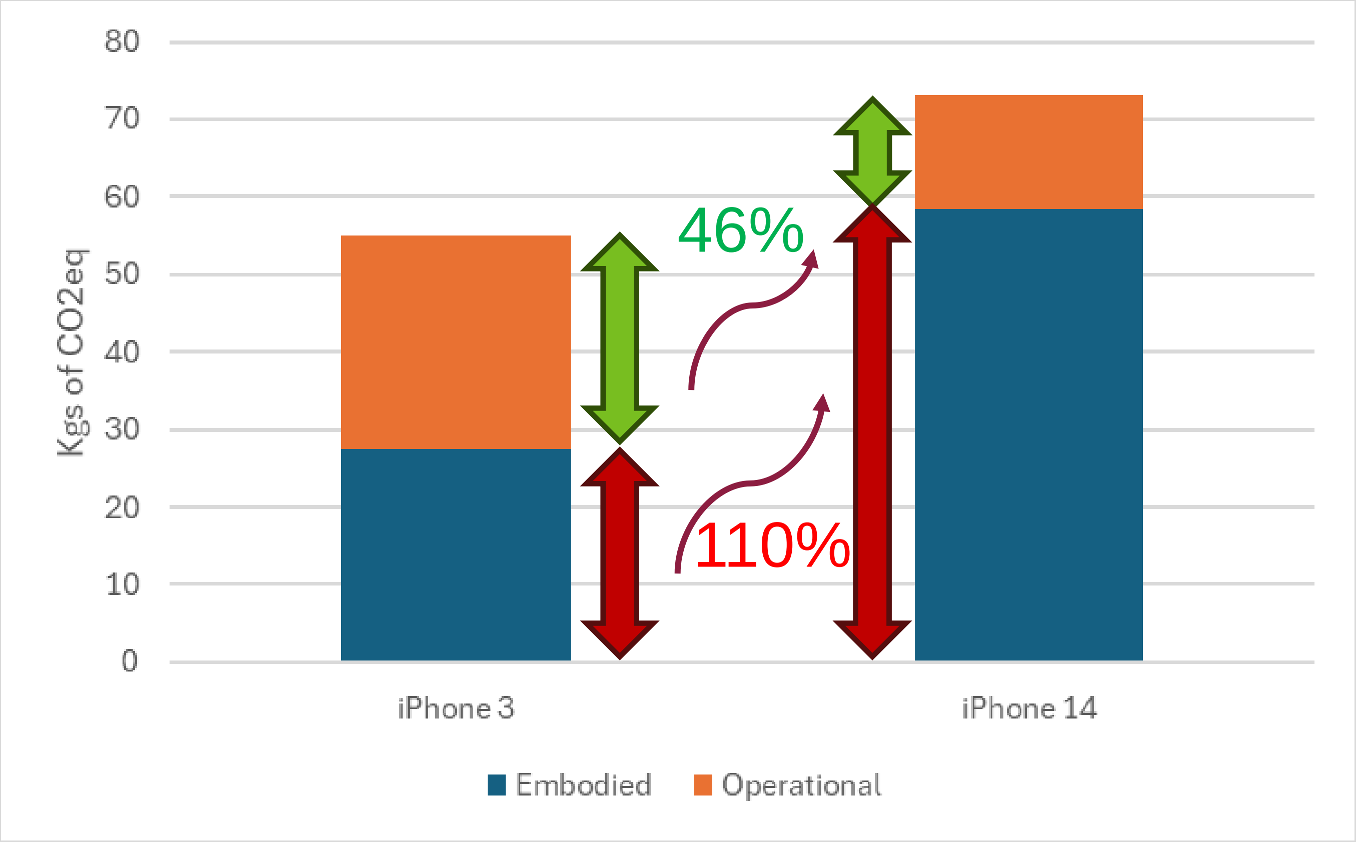


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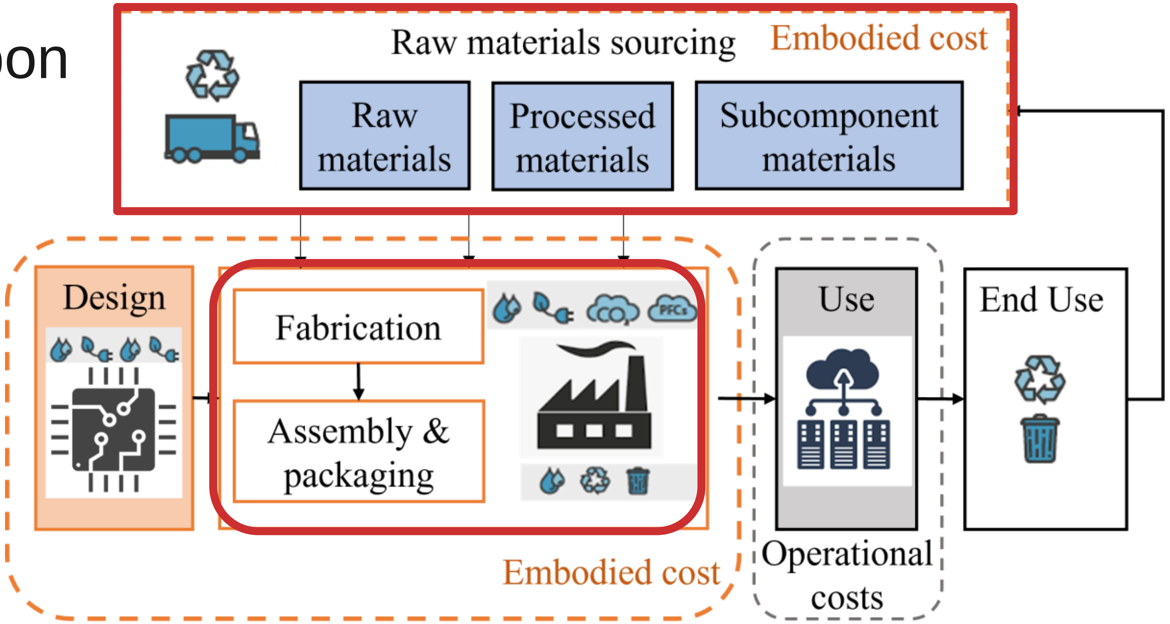
- Architectural model estimating embodied carbon
- Based on industry reports



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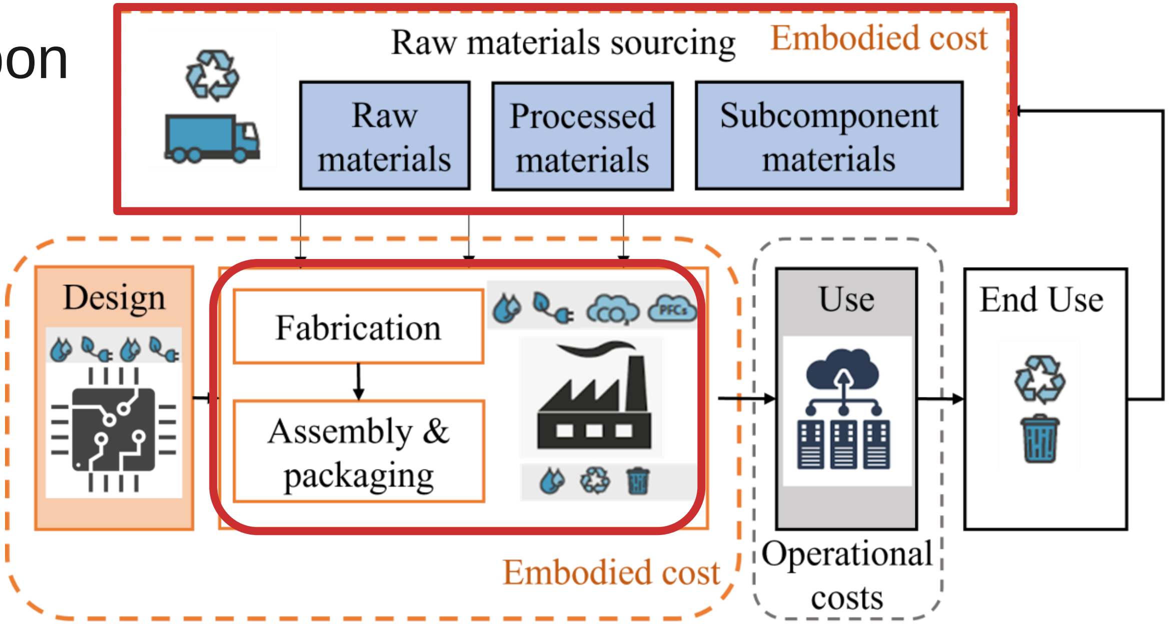


**ECO-CHIP** [*HPCA 2024*]

- Proposes heterogeneous integration as a pathway toward sustainability
- Estimates design and multiple advanced packaging architecture CFP
- Framework also evaluates operational CFP

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Reconfigure for multiple applications

Long lifetime

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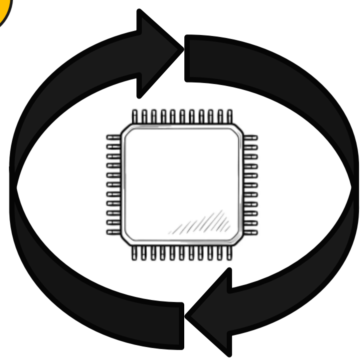

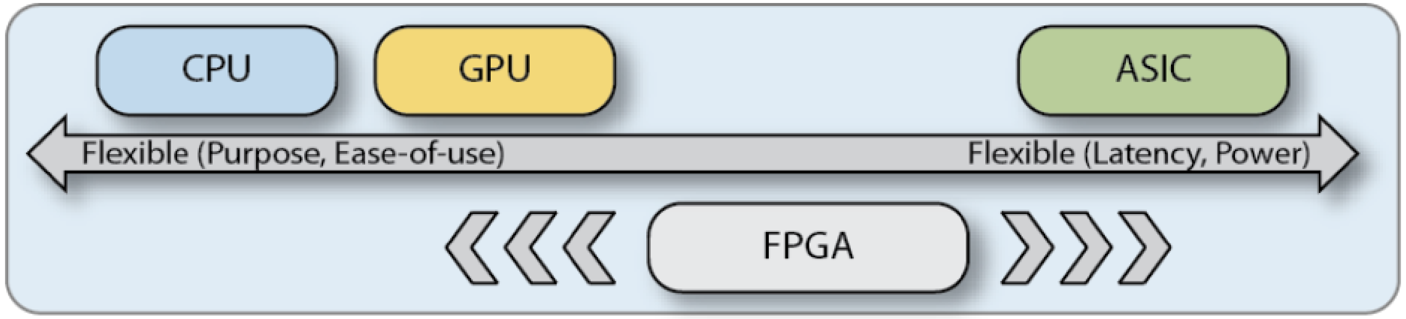

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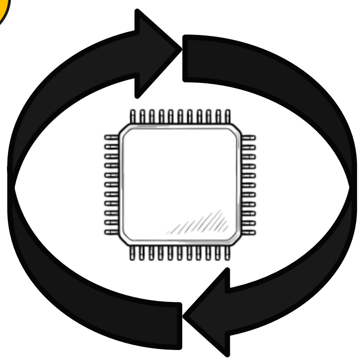

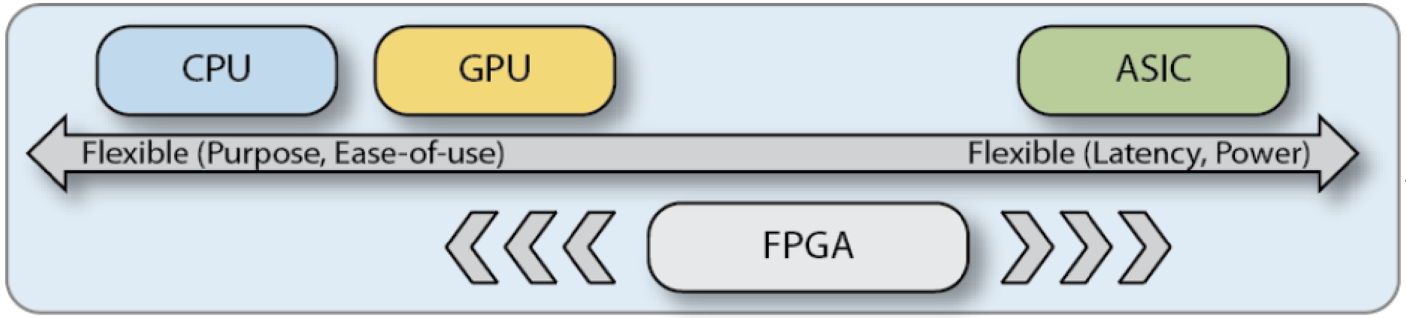


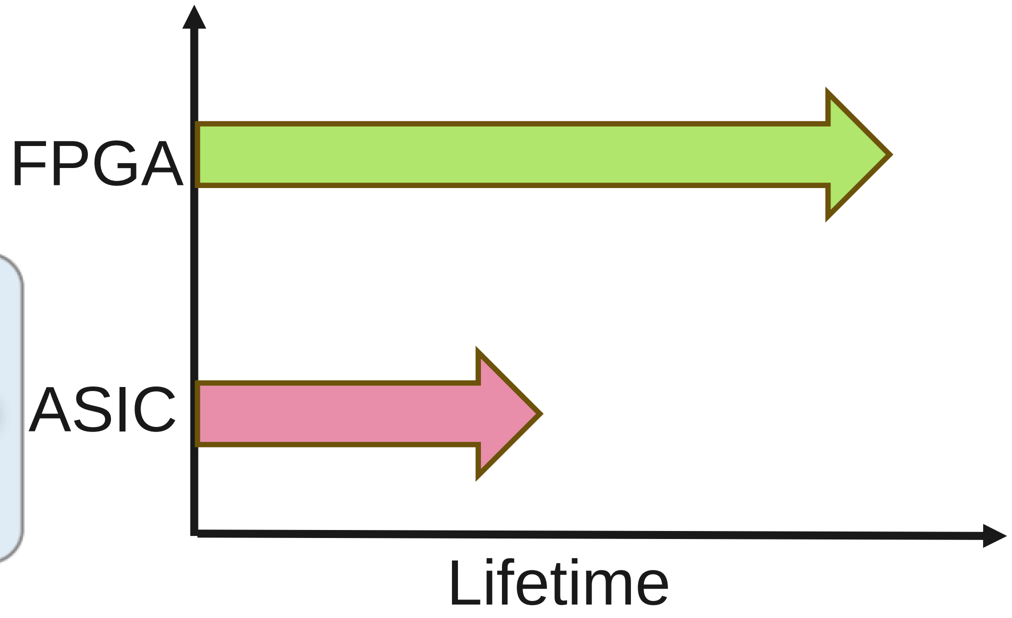

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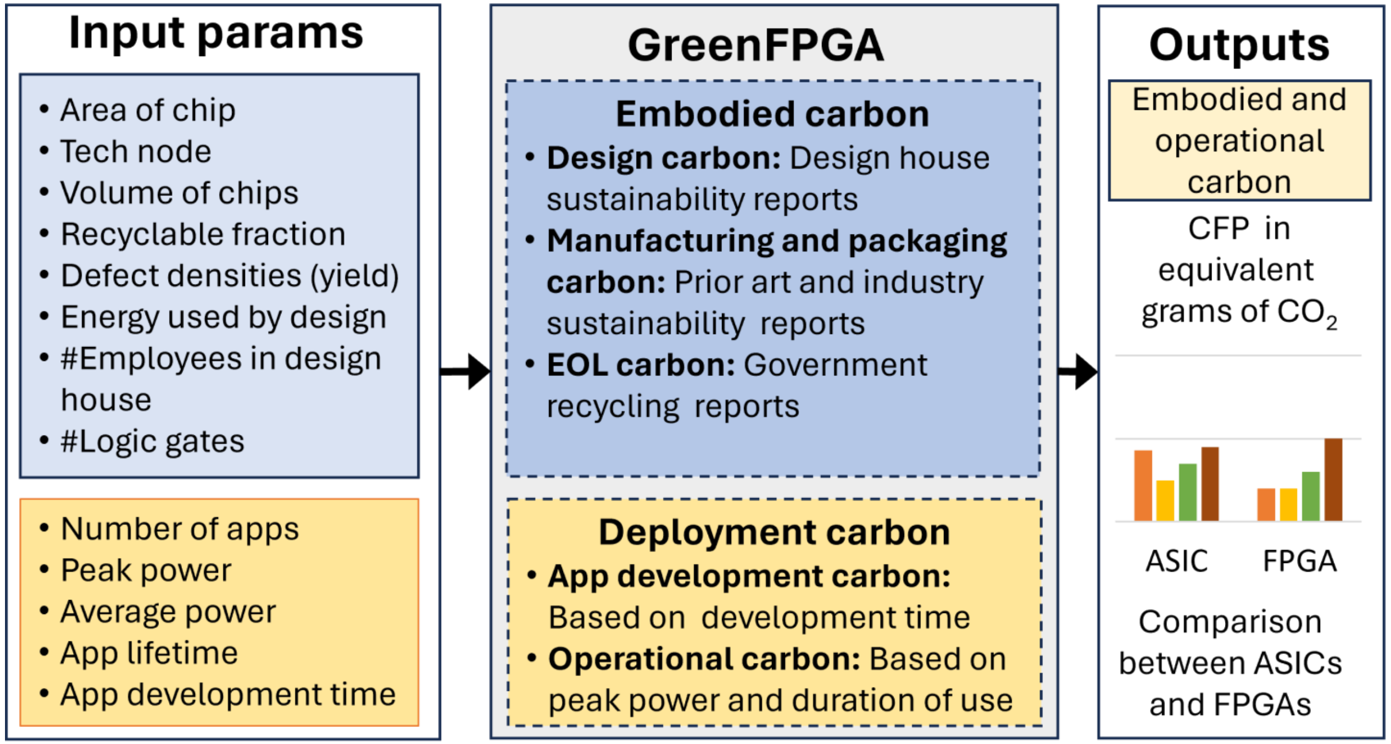

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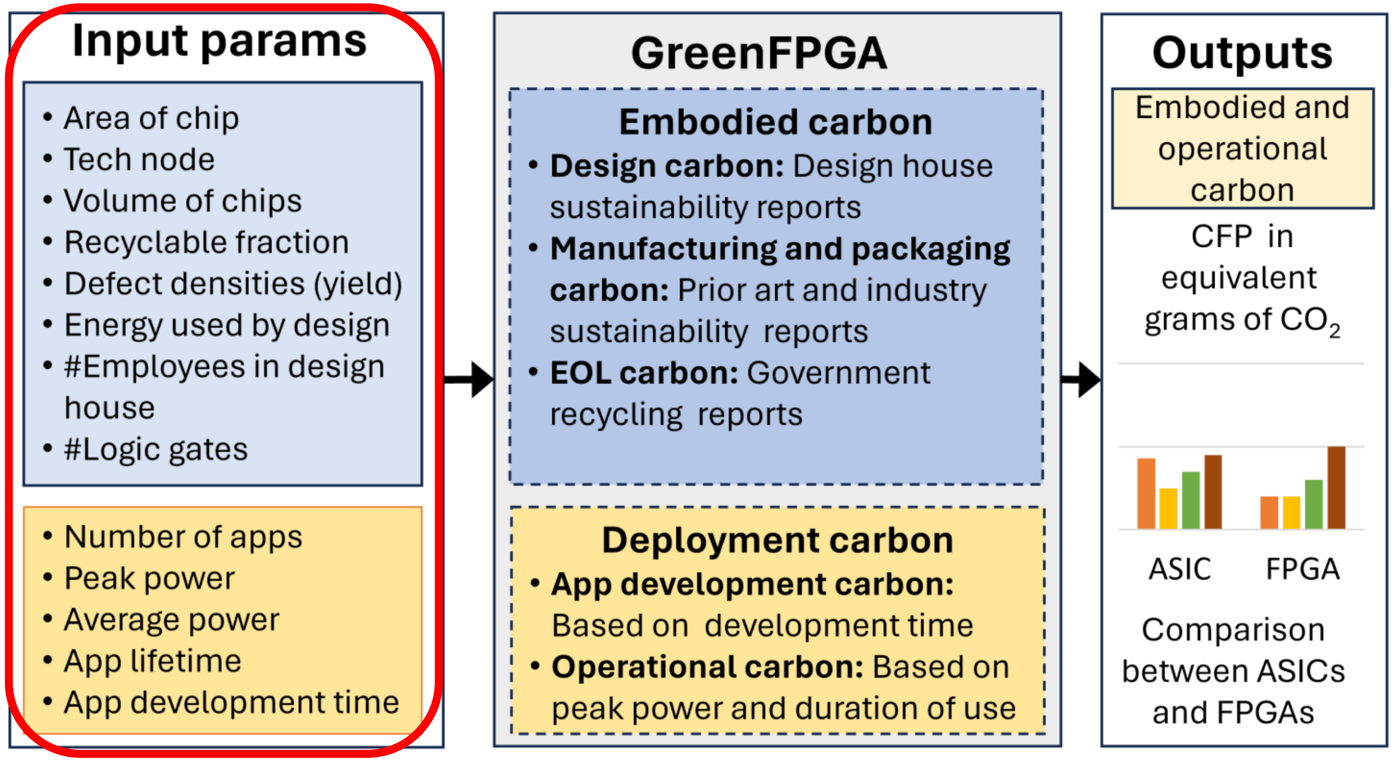

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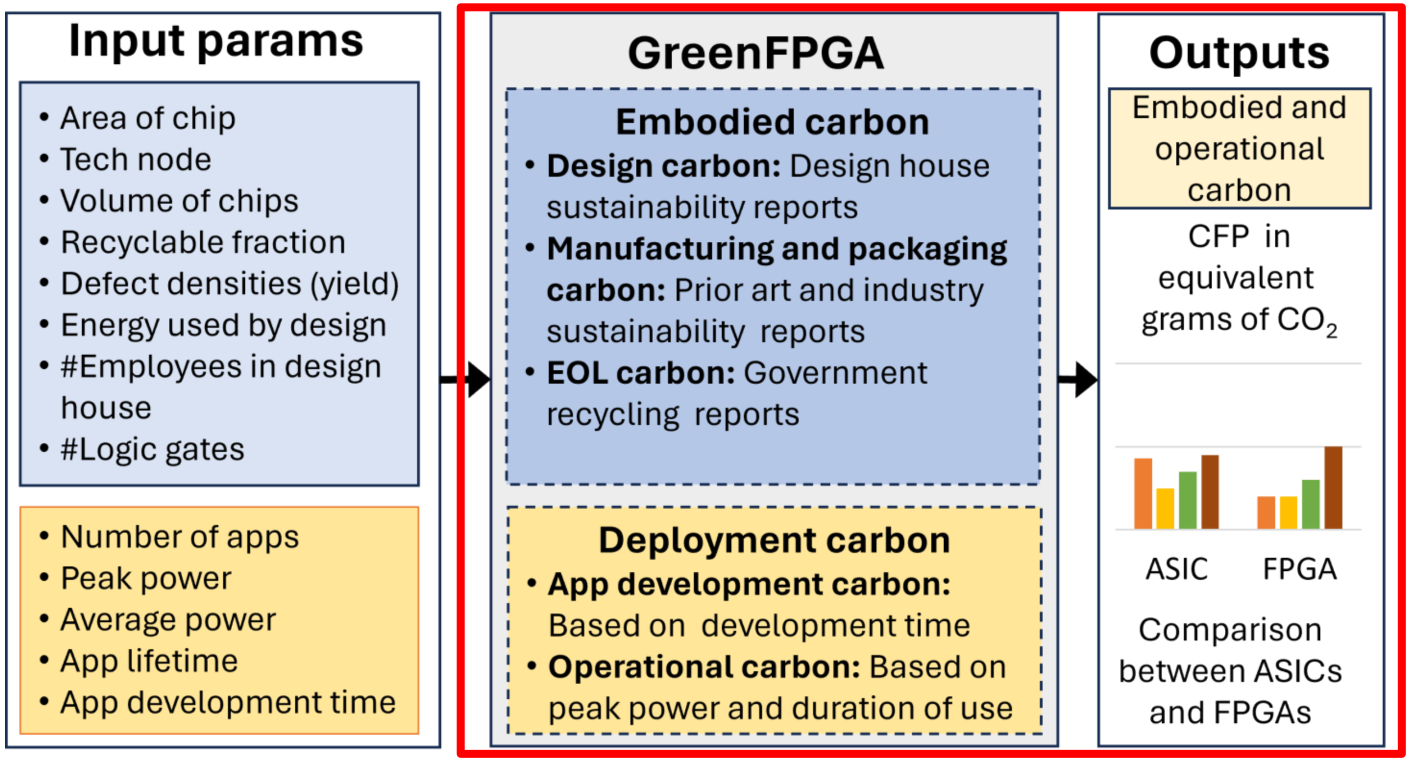

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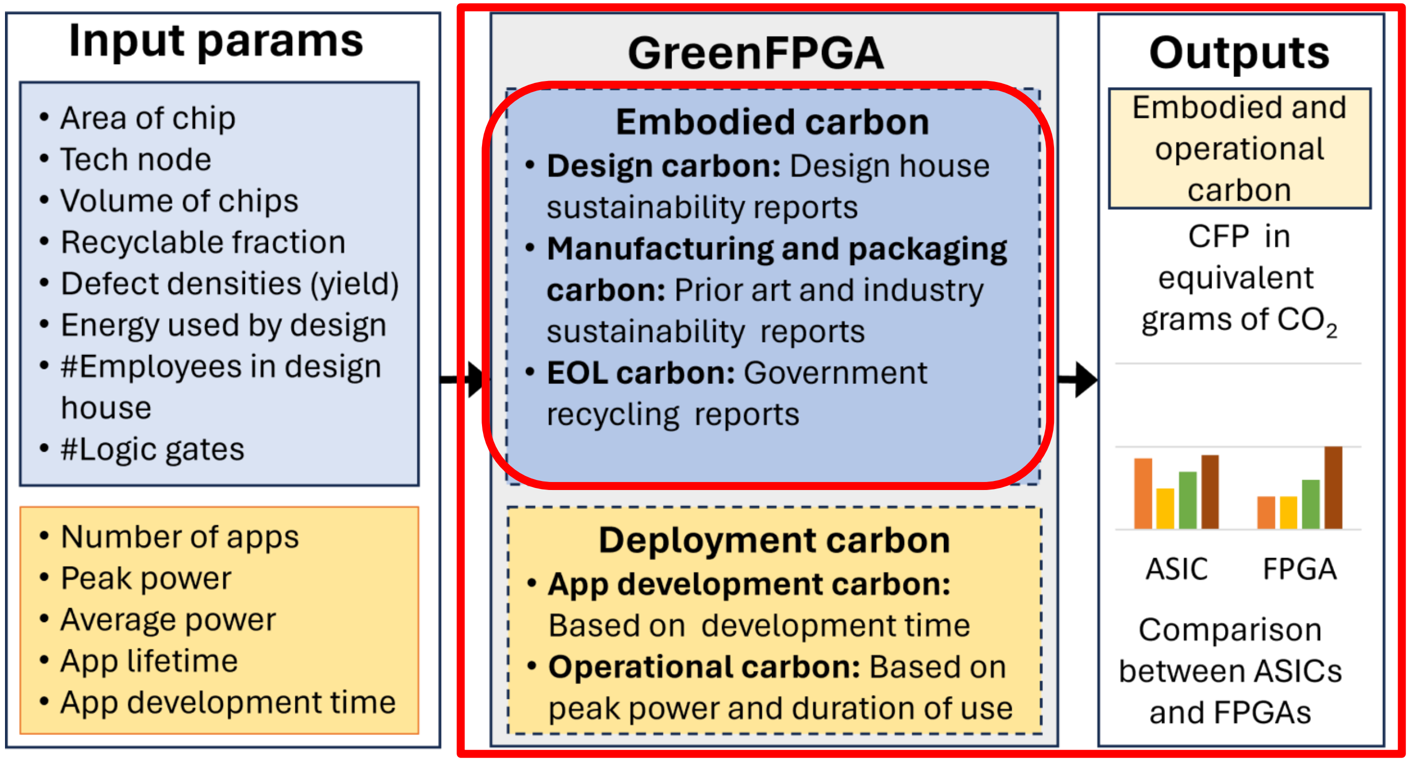

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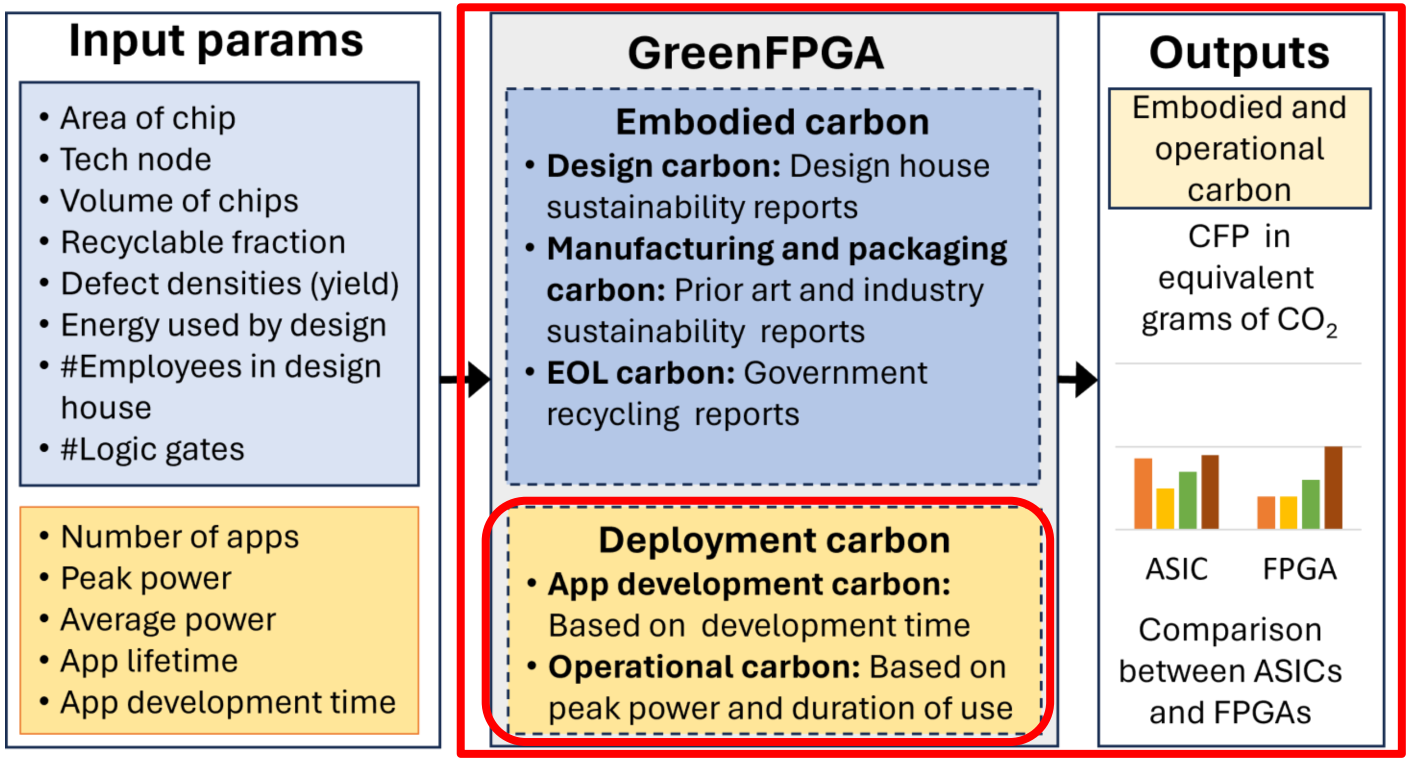

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The total carbon for an FPGA ($C_{FPGA}$) is given by the equation below

$$C_{FPGA} = C_{emb} + \sum_{i=1}^{i=N_{app}} T_i \times C_{deploy,i}$$

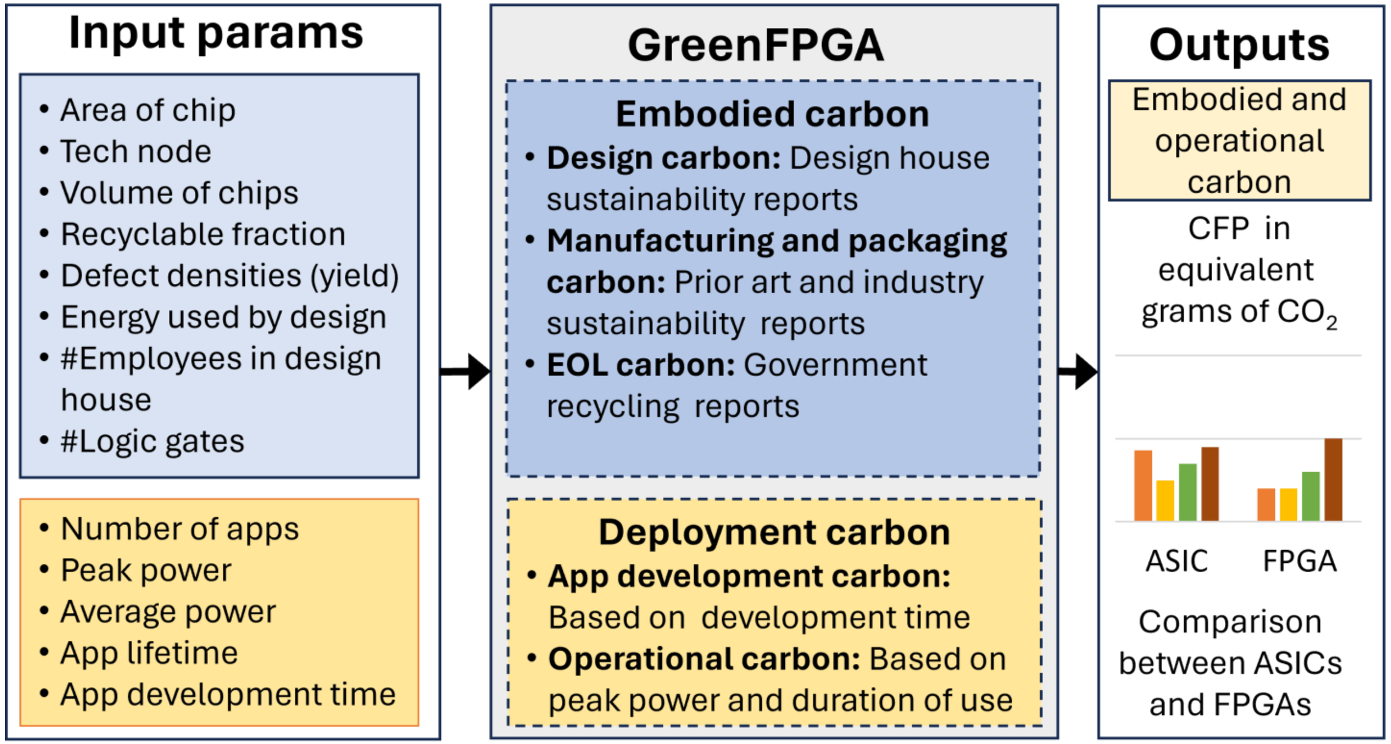
$$C_{ASIC} = \sum_{i=1}^{i=N_{app}} (C_{emb,i} + T_i \times C_{deploy,i})$$

$C_{FPGA}$ - Total FPGA CFP

$C_{emb}$ - Embodied carbon

$C_{deploy}$ - Deployment carbon

$N_{app}$ - Total number of applications



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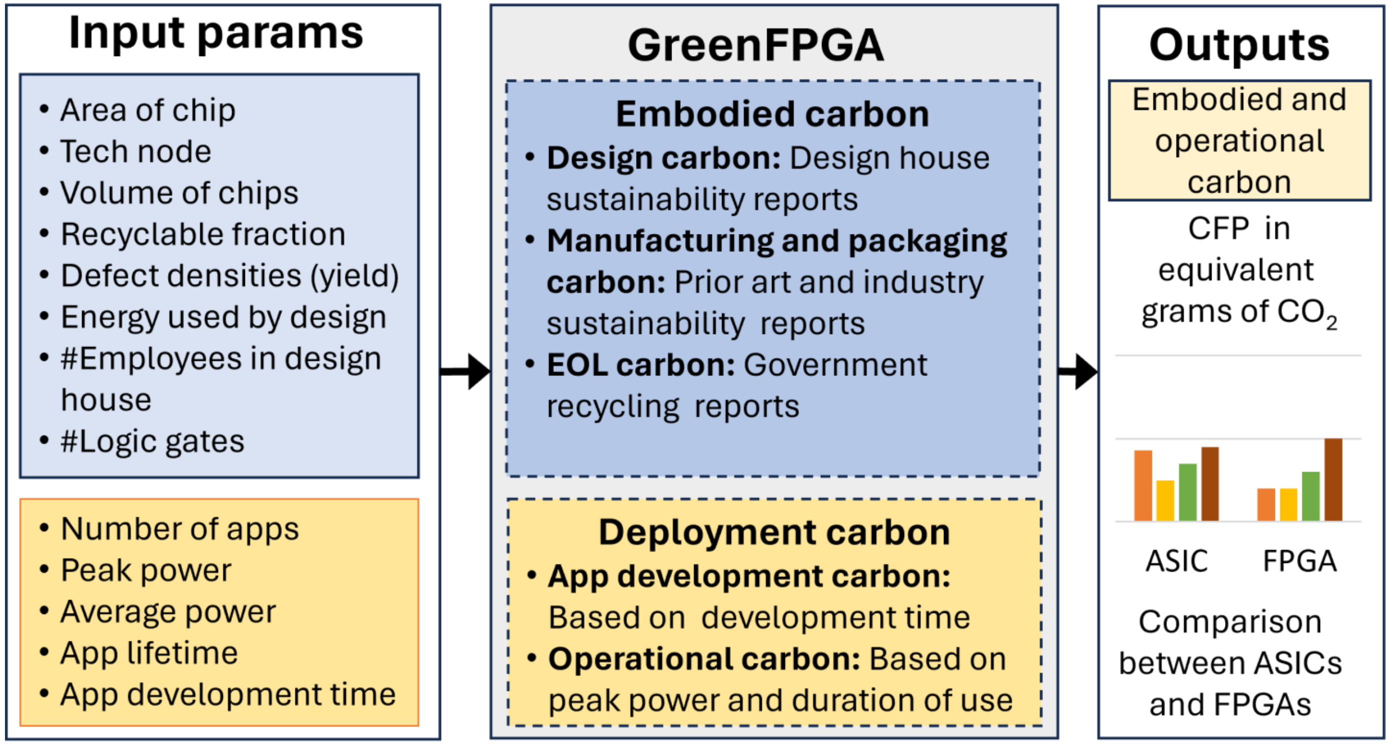


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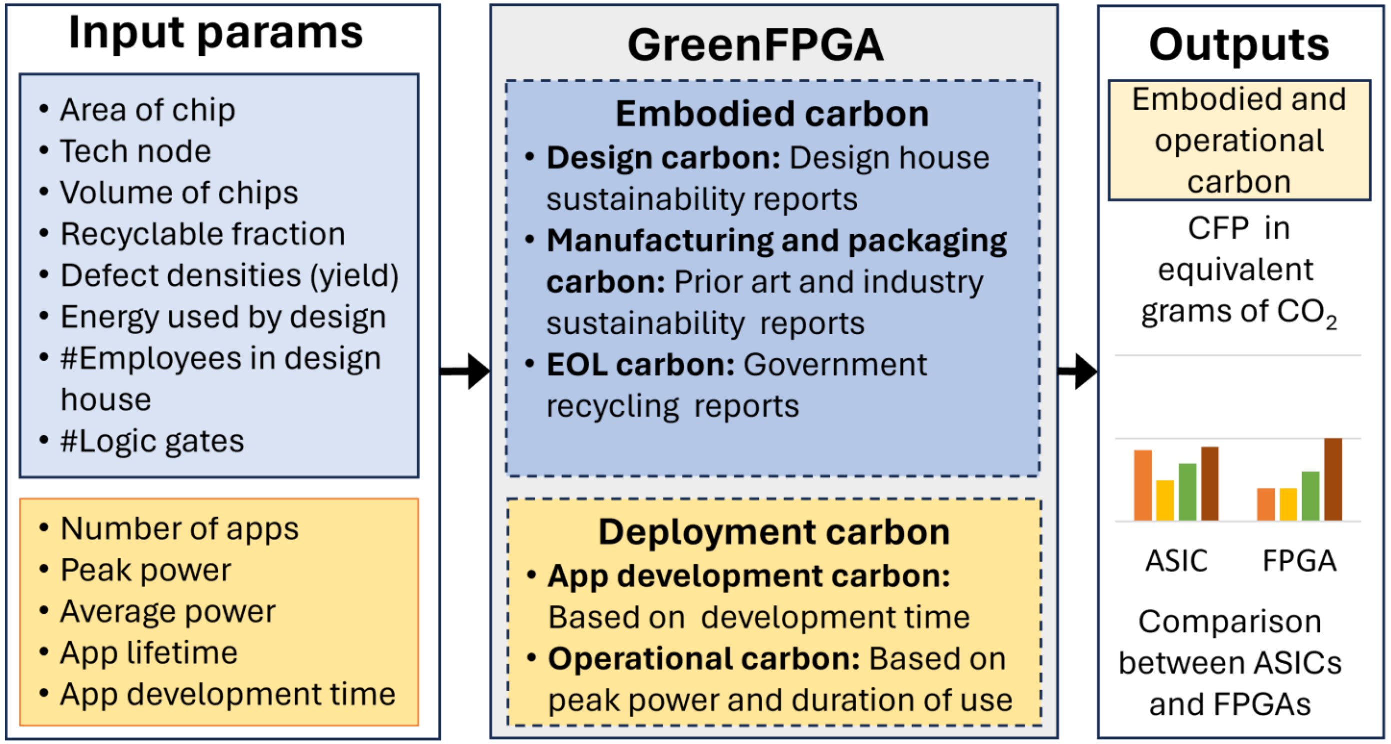

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$$C_{emb} = C_{des} + \left(N_{vol} \times N_{FPGA} \times \left(C_{mfg} + C_{pkg} + C_{EOL}\right)\right)$$

$C_{des}$ = Design carbon

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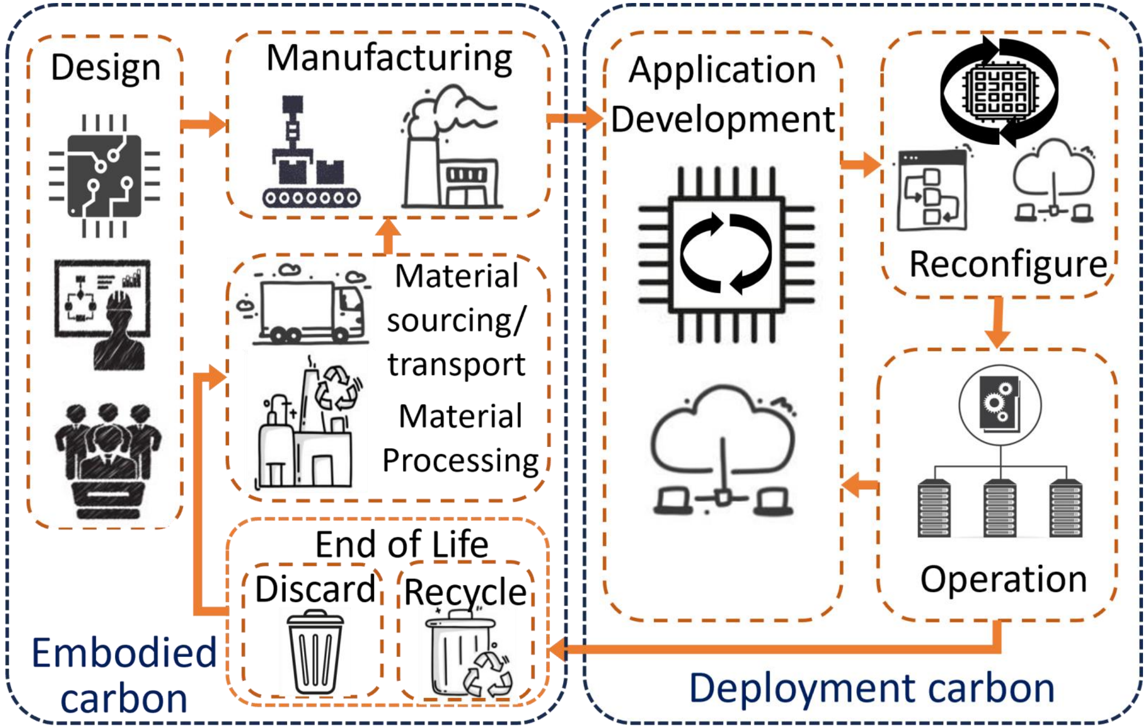

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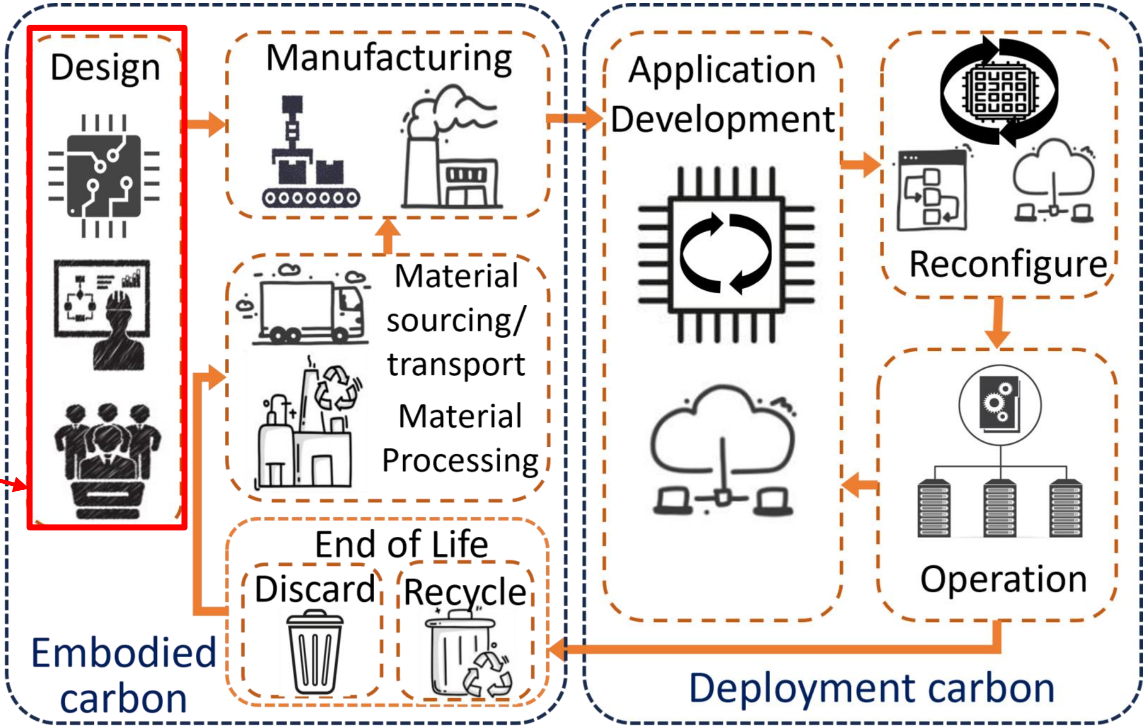

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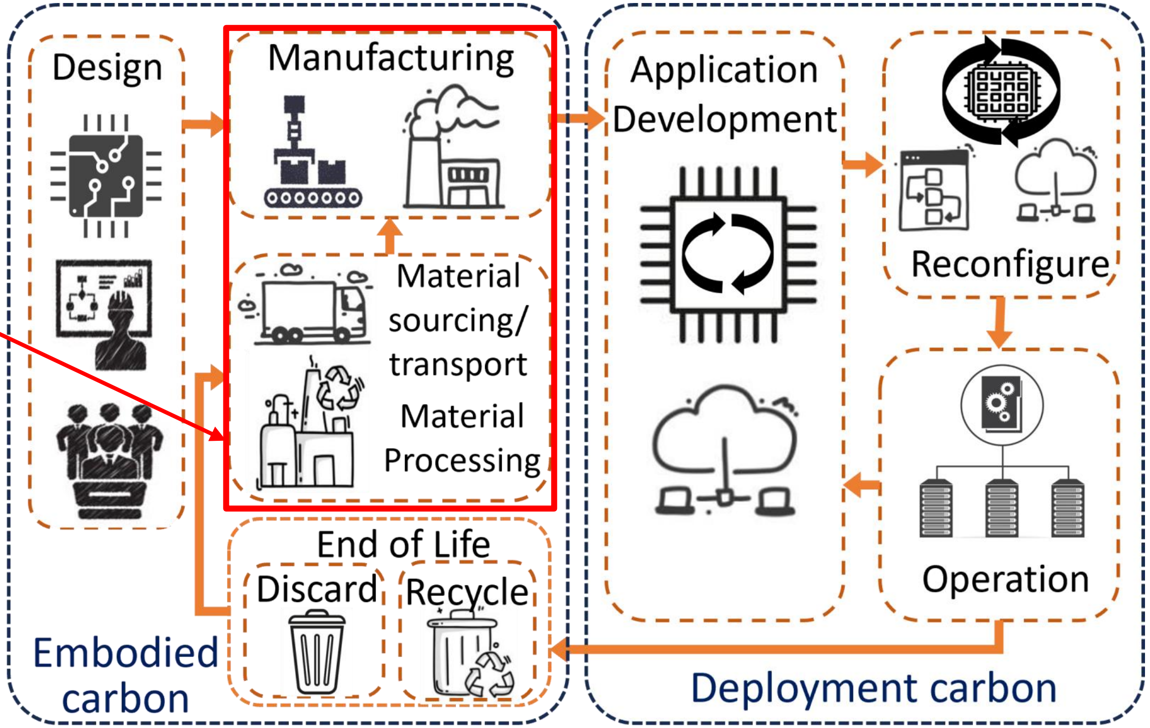


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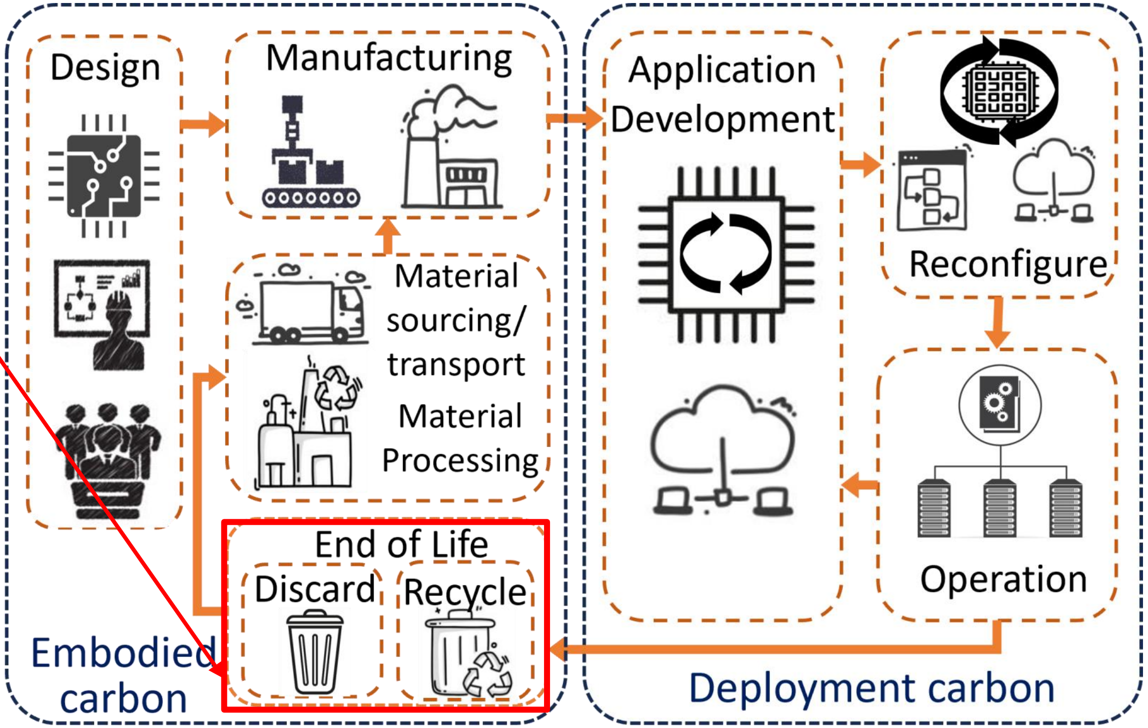

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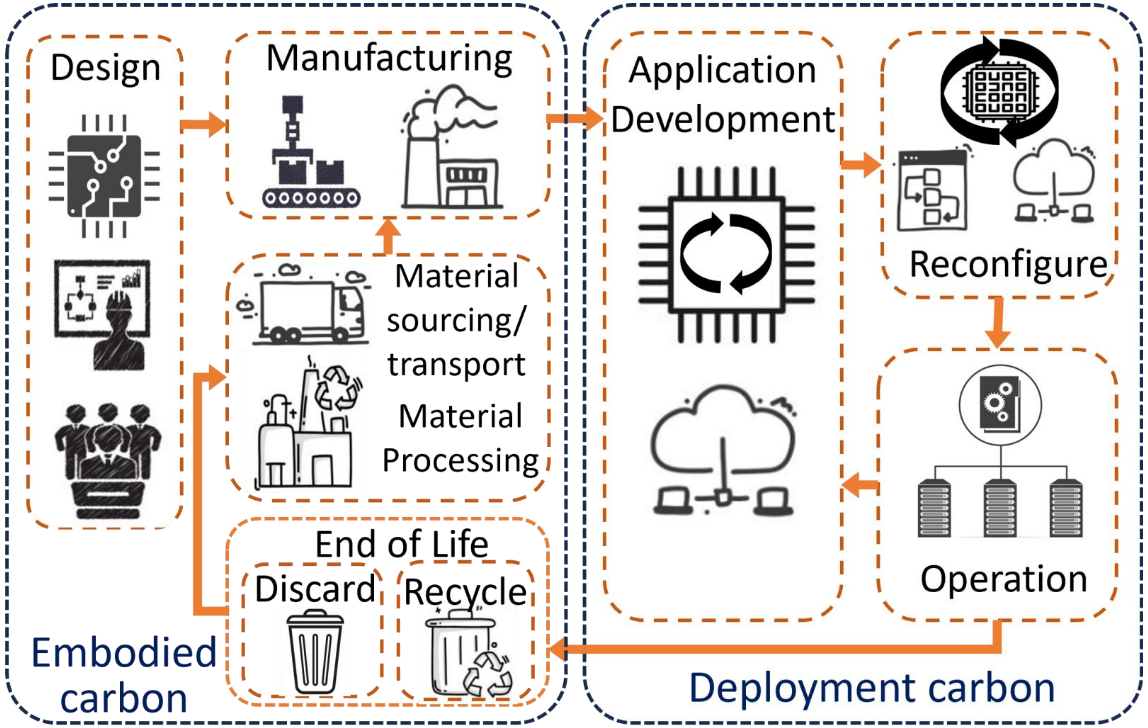

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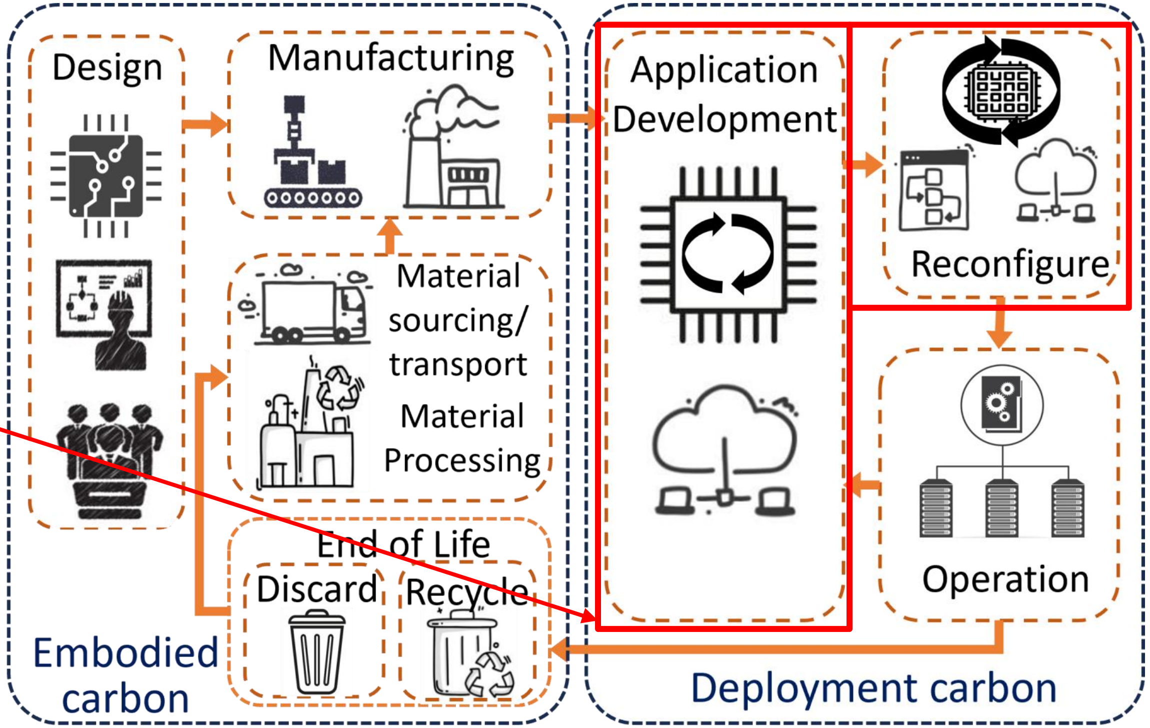

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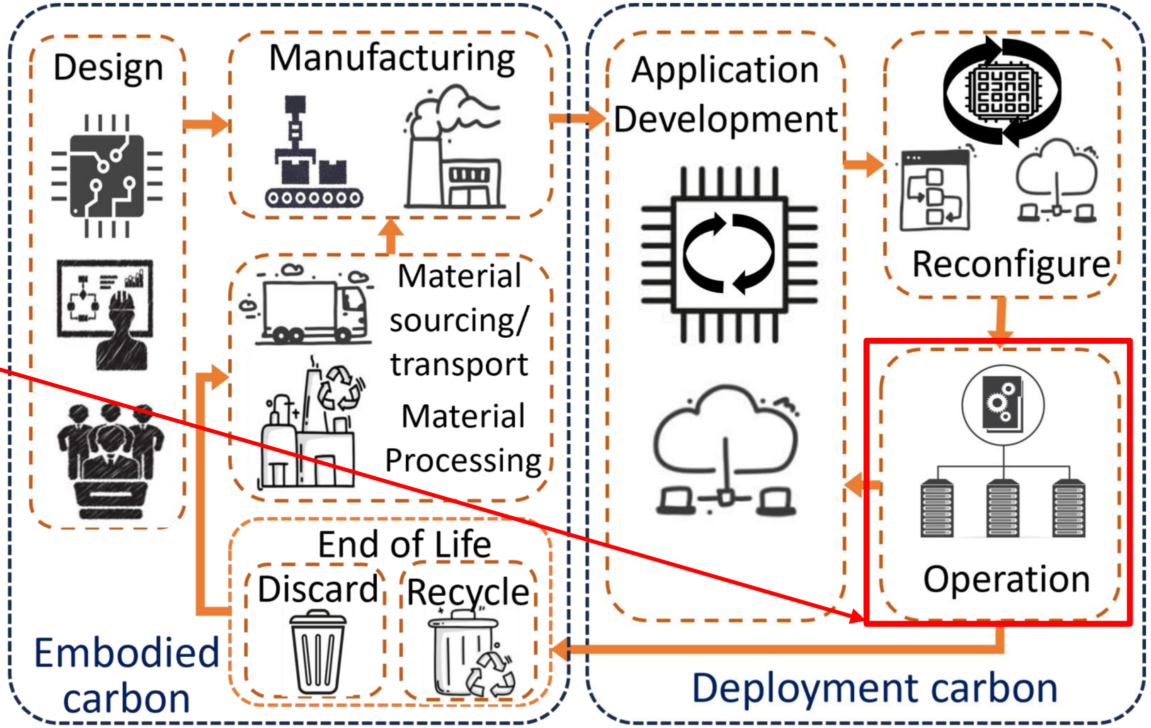

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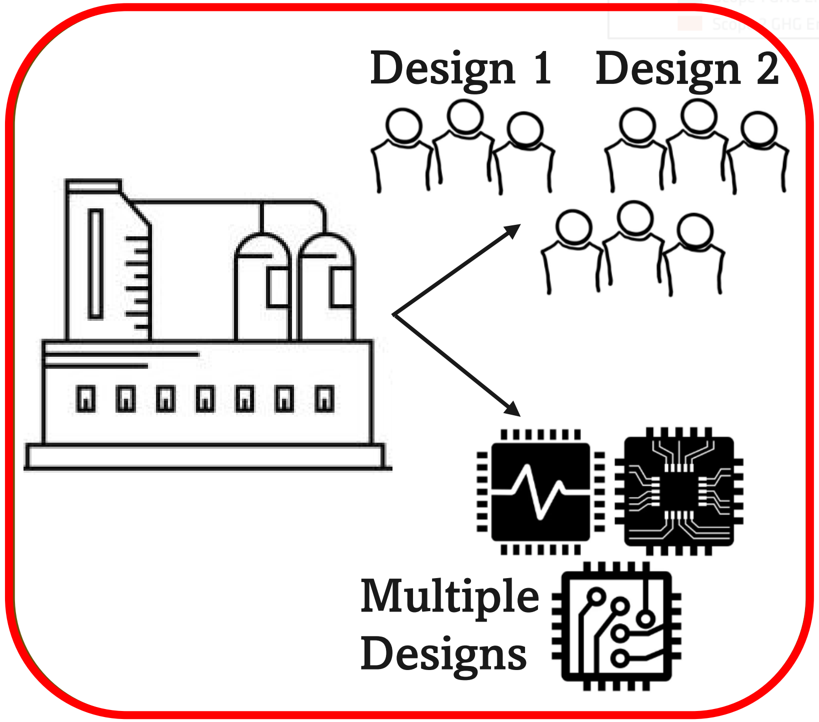


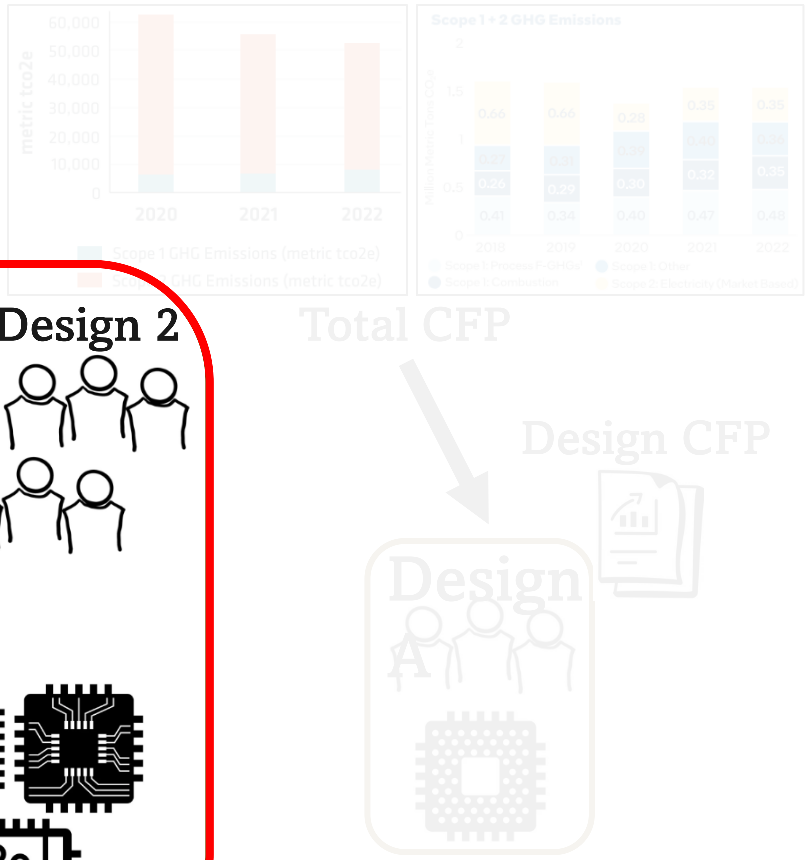

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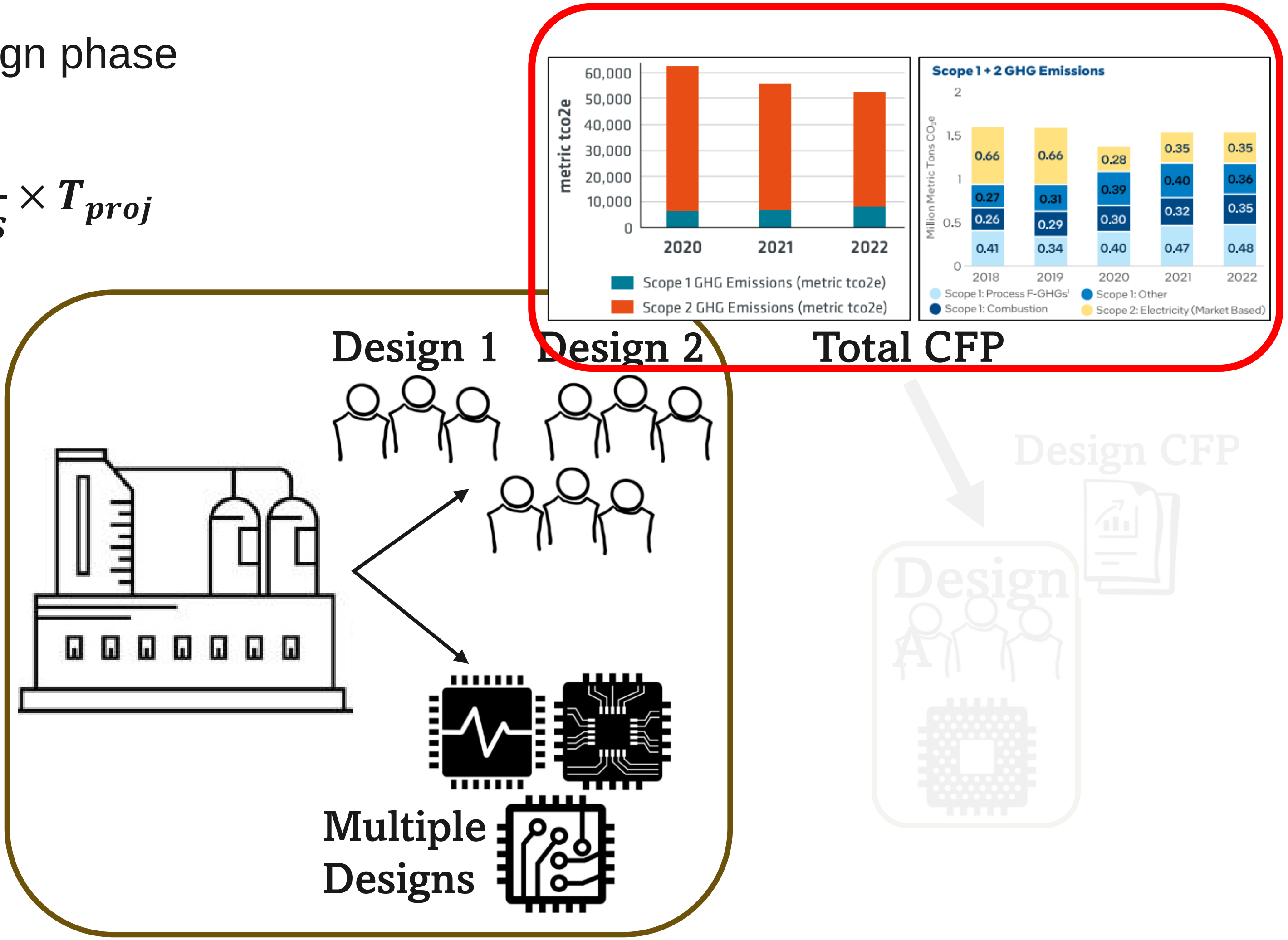

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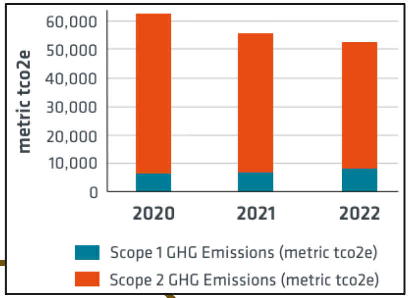


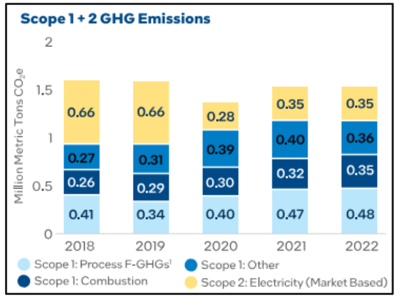


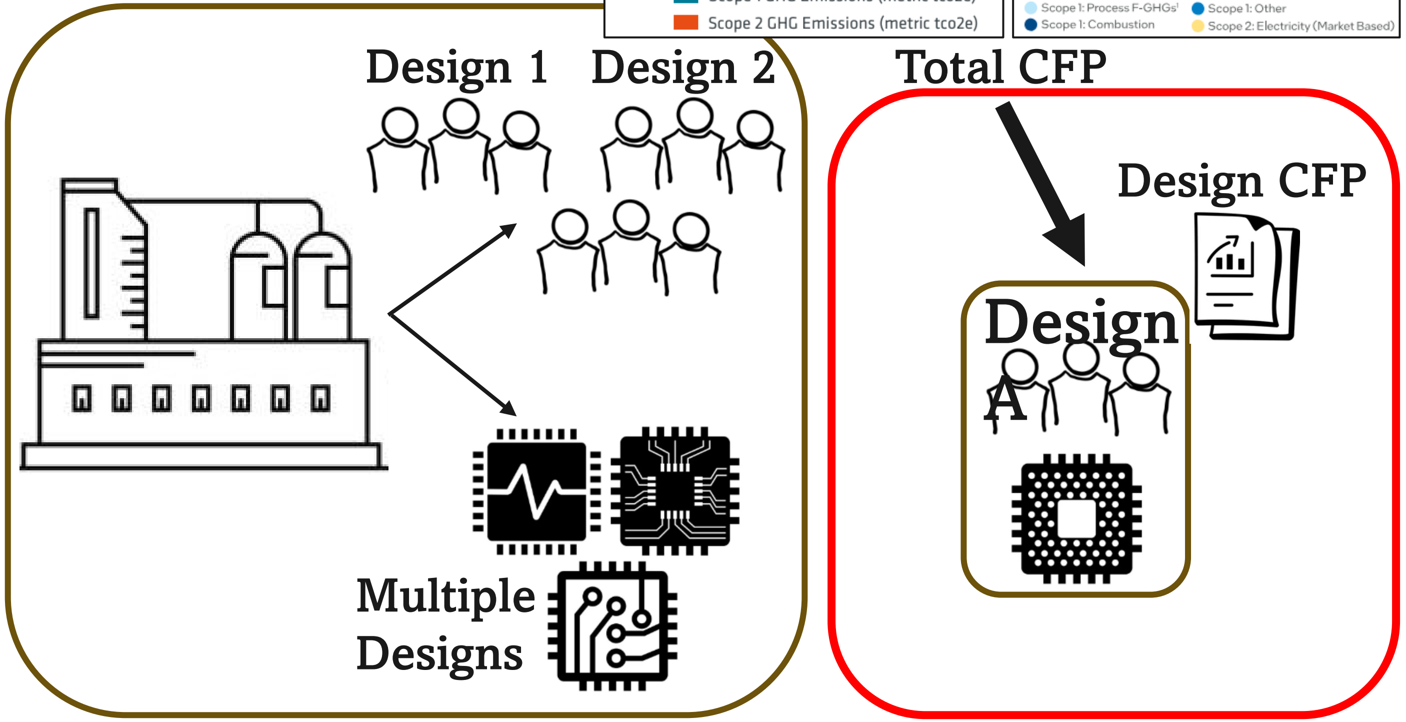

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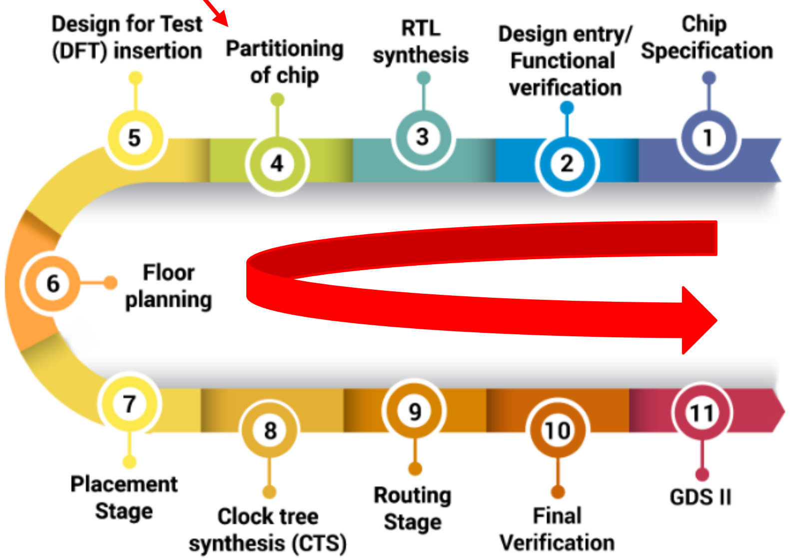


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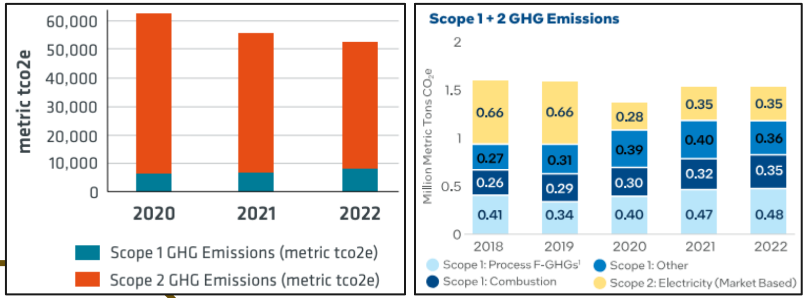


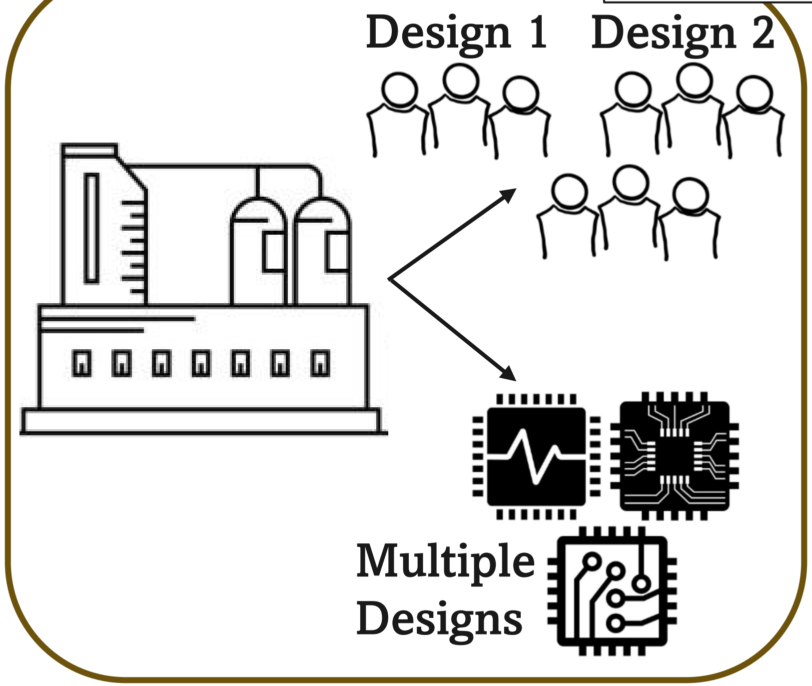


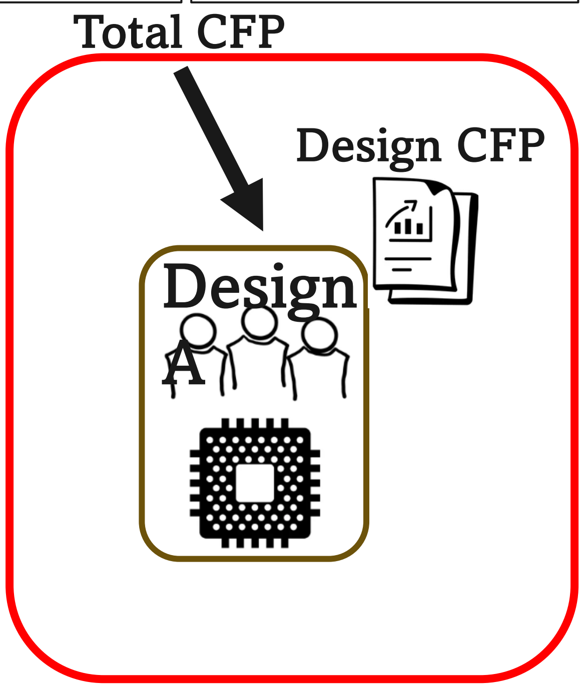

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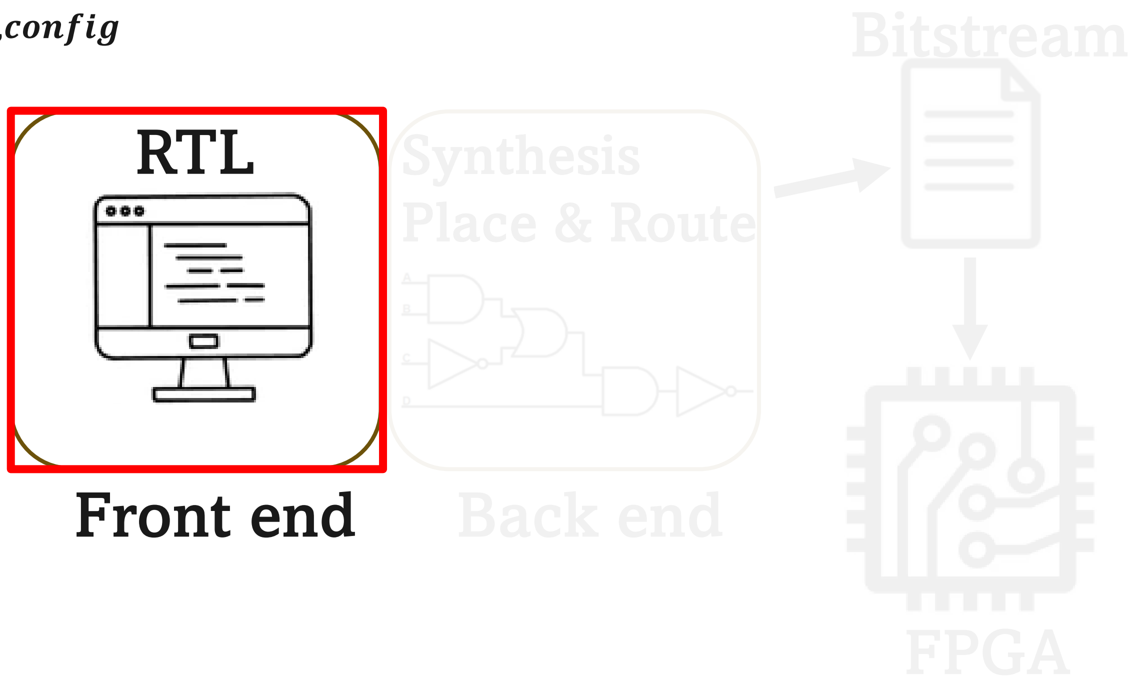

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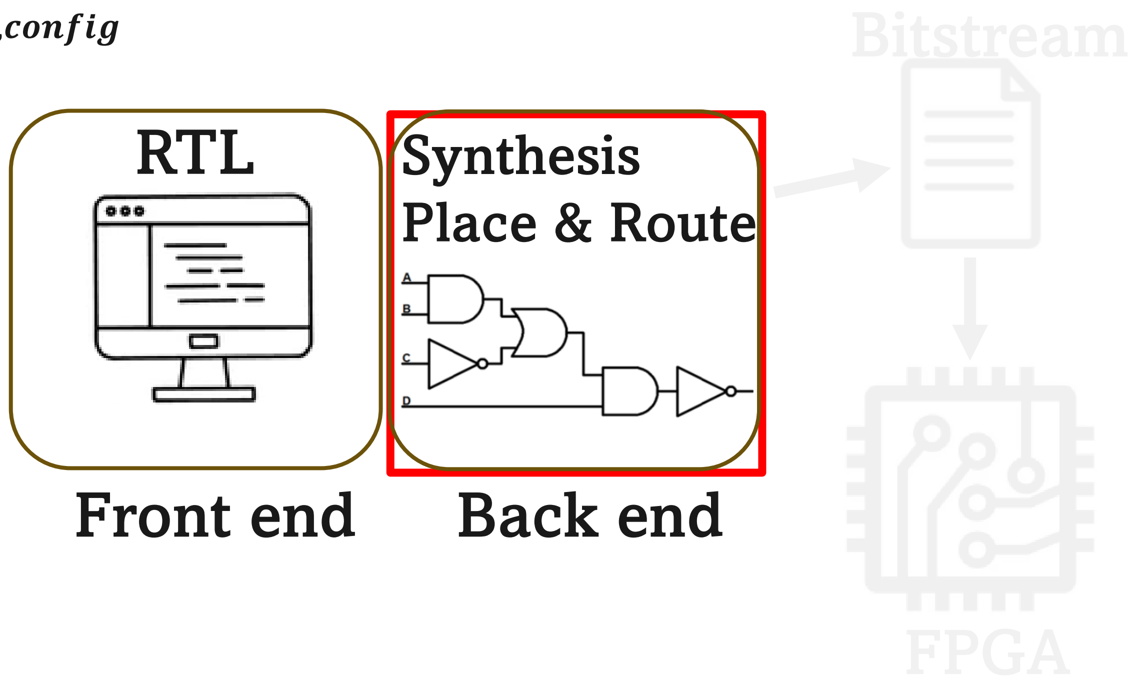
$$T_{app-dev} = N_{app} \times (front + back\ end\ dev) + N_{vol} \times T_{app,config}$$



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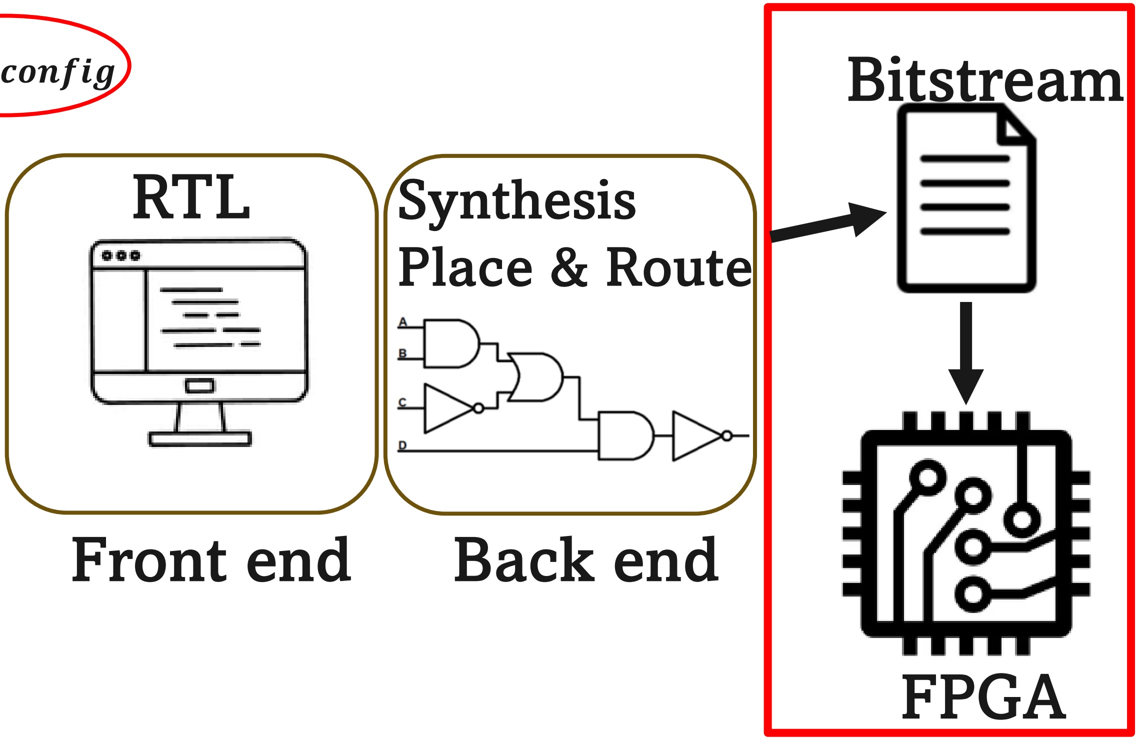

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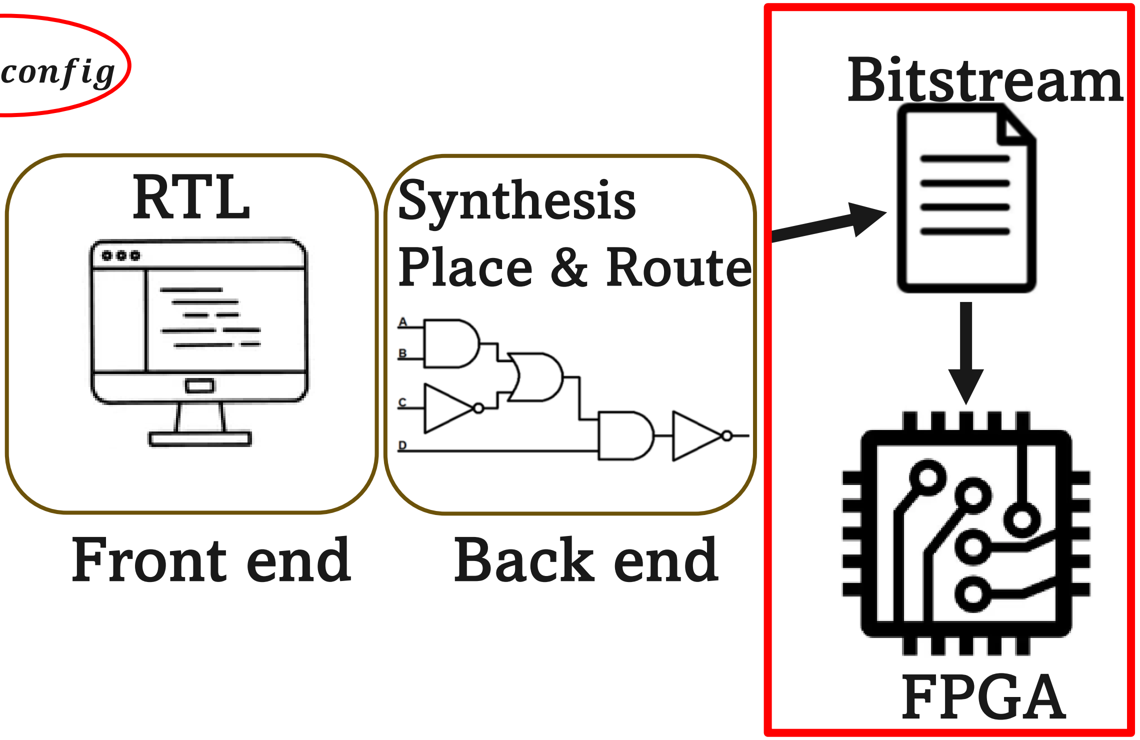
$$T_{app-dev} = N_{app} \times (front + back\ end\ dev) + N_{vol} \times T_{app,config}$$

Front and back-end development time is done once per application, and then configured on all the FPGAs

$N_{app}$ - Total number of applications
$N_{vol}$ - Application volume
$T_{app,config}$ - Duration of the design project

$$C_{app-dev} = P_{app-dev} \times T_{app-dev} \times C_{src}$$

$P_{app-dev}$ - Power of CPU used for app-dev
$C_{src}$ - Carbon intensity of energy source



# Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- GreenFPGA
  - FPGA as sustainable computing solution
  - GreenFPGA framework
  - GreenFPGA modeling
- **Results and analysis**
- **Conclusion and takeaway**

# GreenFPGA results and analysis

- Compare ASIC to FPGAs at iso-performance
- Analyzed for three application domains
  - Deep neural networks (DNN)
  - Image processing (ImgProc)
  - Cryptography (Crypto)

| Testcases | Crypto | ImgProc | DNN |
|---|---|---|---|
| Area (normalized to ASIC) | 1 | 7.42 | 4 |
| Power (normalized to ASIC) | 1 | 1.25 | 3 |

Source : T. Tan's PhD dissertation, 2023

- [T. Tan,2023] emphasizes that ASICs are designed for architectural application and lack reconfigurability and flexibility.
- FPGAs are highly reconfigurable with the ability to be tuned for specific application

# Analysis: Number of applications

| Testcases | Crypto | ImgProc | DNN |
|---|---|---|---|
| Area (normalized to ASIC) | 1 | 7.42 | 4 |
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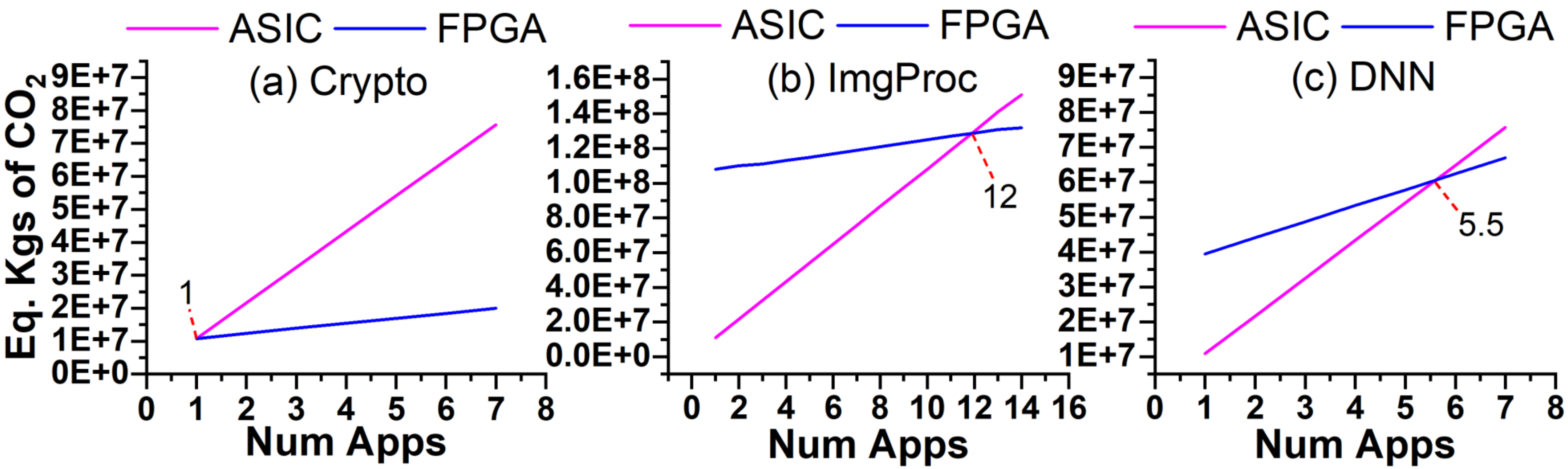


- Number of applications swept keeping volume and application lifetime constant
- Compared ASIC and FPGA for iso-performance
- Power and area variations for different application domains impact A2F cross over point

# Analysis: Application lifetime

| Testcases | Crypto | ImgProc | DNN |
|---|---|---|---|
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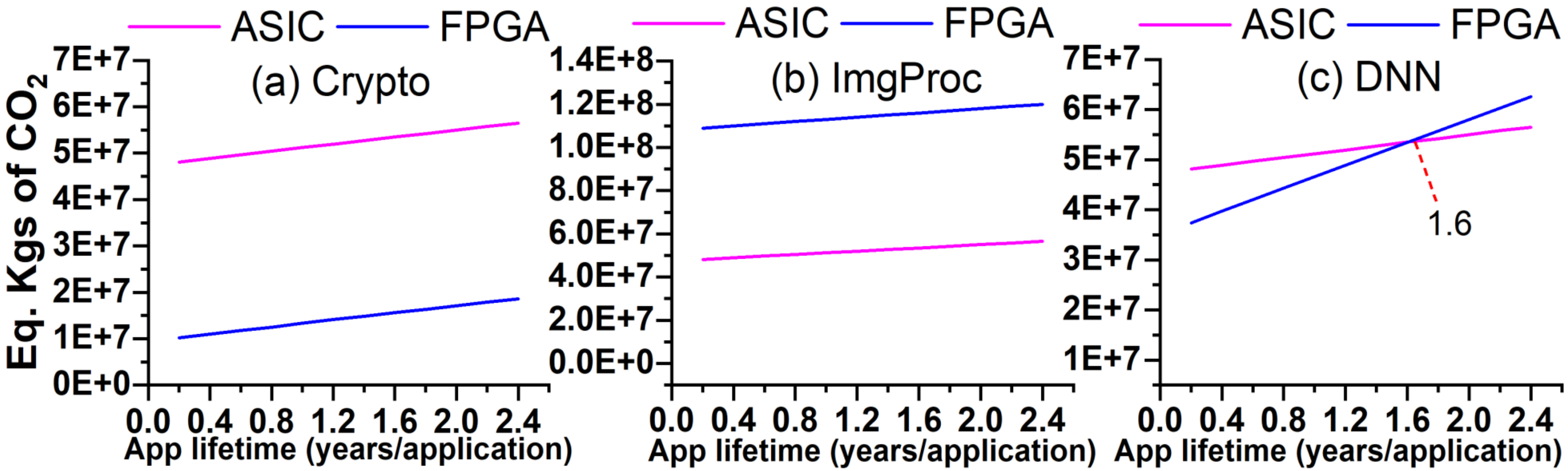
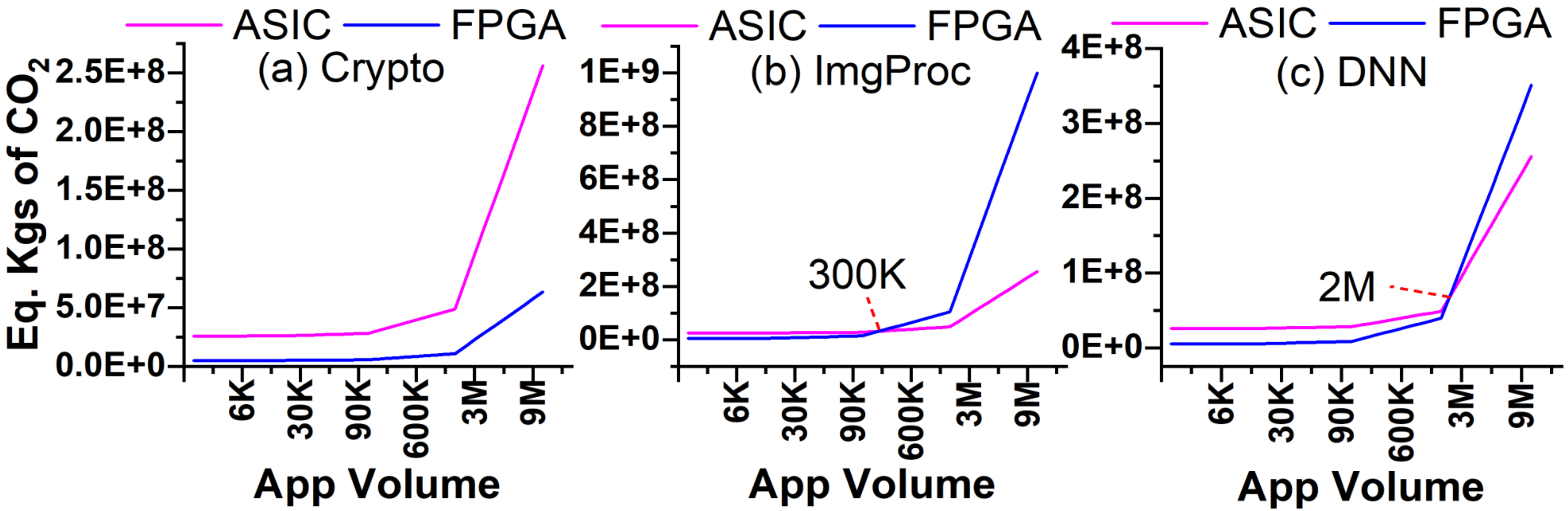



- Application lifetime swept keeping number of application and volume constant
- Image processing ASIC is better due to lower power and area
- FPGA sustainable for DNN applications for shorter lifetime with F2A point at 1.6 years

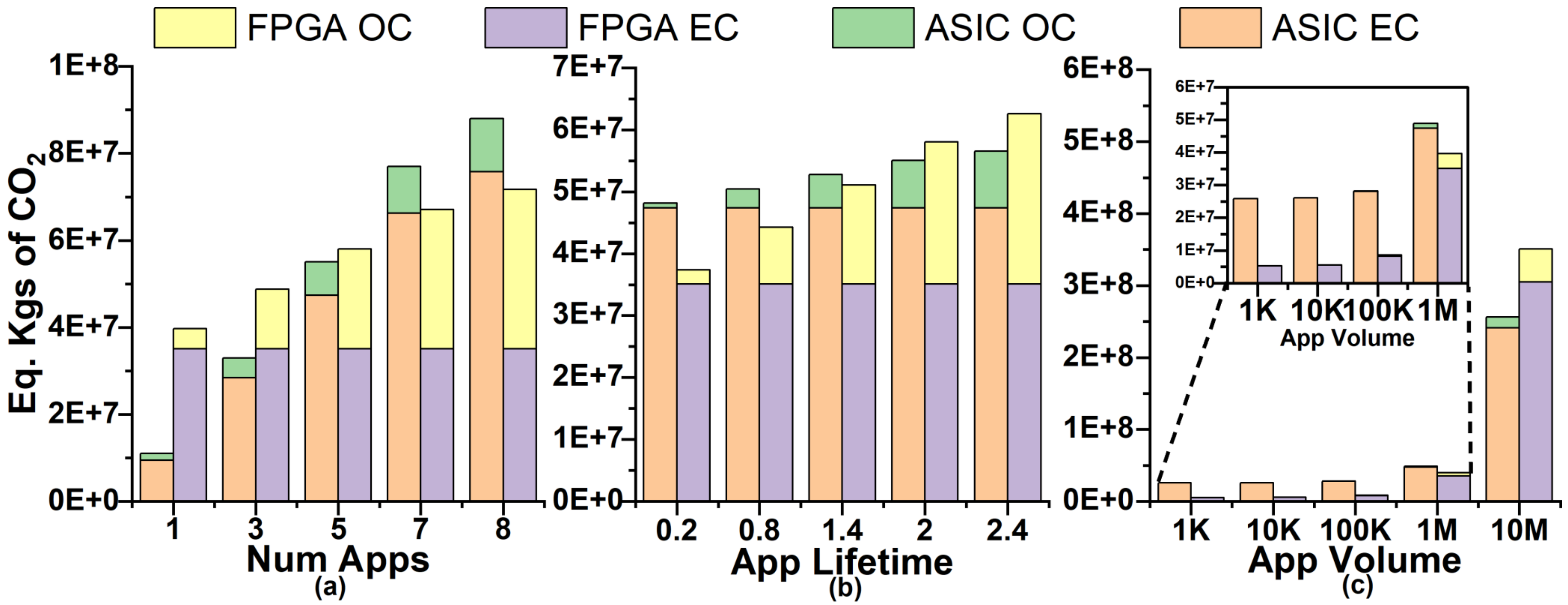
# Analysis: Application volume

| Testcases | Crypto | ImgProc | DNN |
|---|---|---|---|
| Area (normalized to ASIC) | 1 | 7.42 | 4 |
| Power (normalized to ASIC) | 1 | 1.25 | 3 |



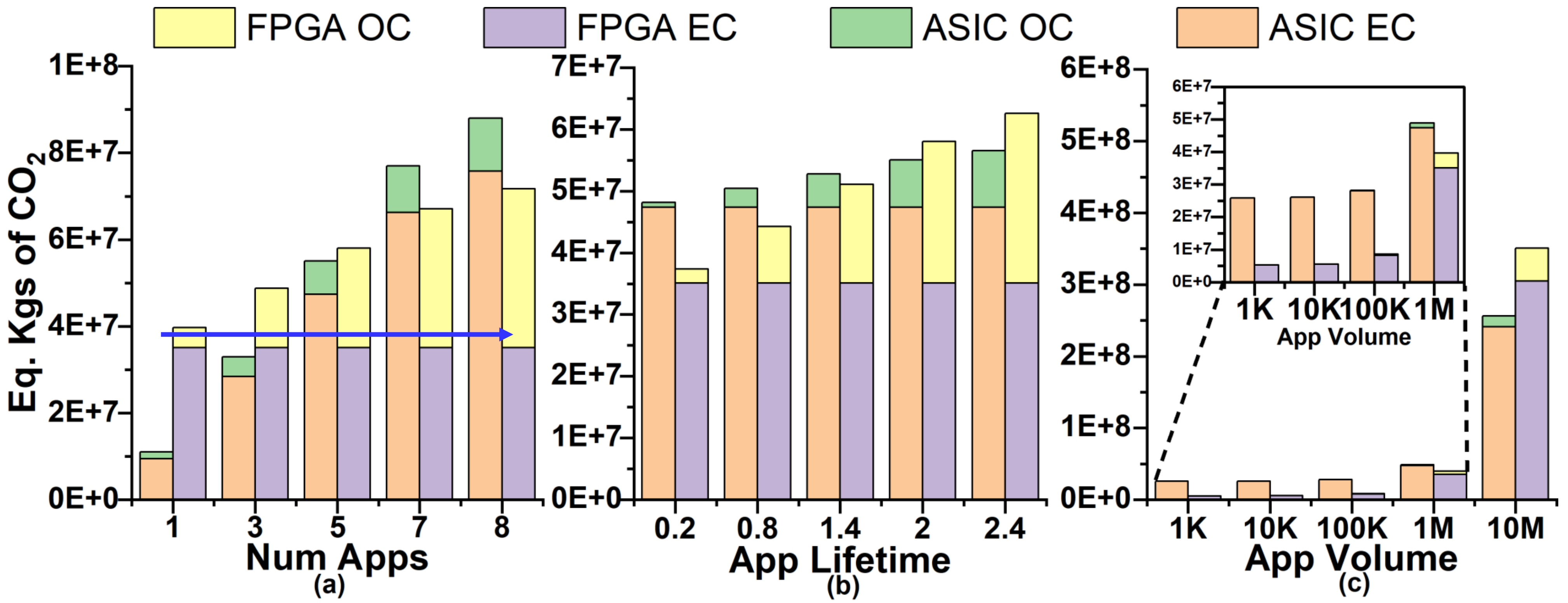

- Application volume swept keeping the number of applications and application lifetime constant
- FPGA is environmentally sustainable for lower application volume
- F2A crossover point determined by power and area variation for iso-performance

# Analysis: CFP components for DNN testcase




- Embodied CFP of FPGA stays the same, while that of ASIC increases as the number of applications increase
- Increase in operational CFP of ASIC is lesser compared to FPGA as application lifetime increases

# Analysis: CFP components for DNN testcase

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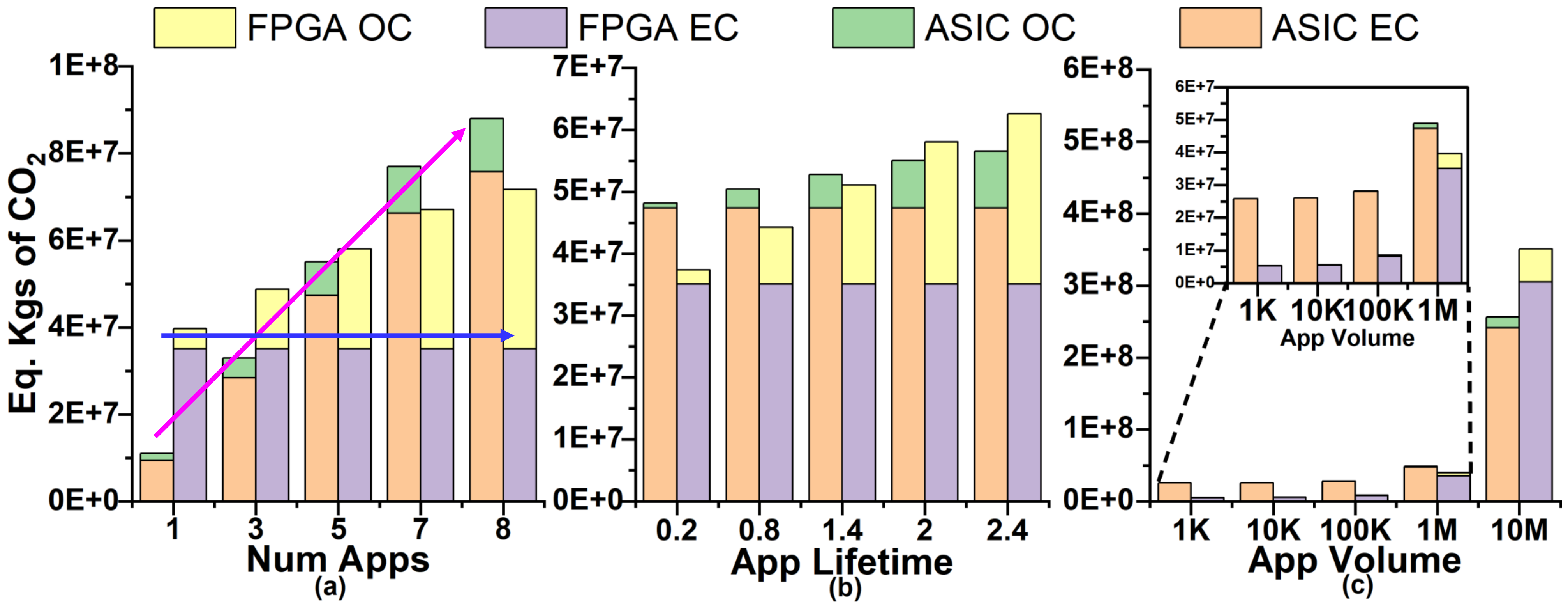


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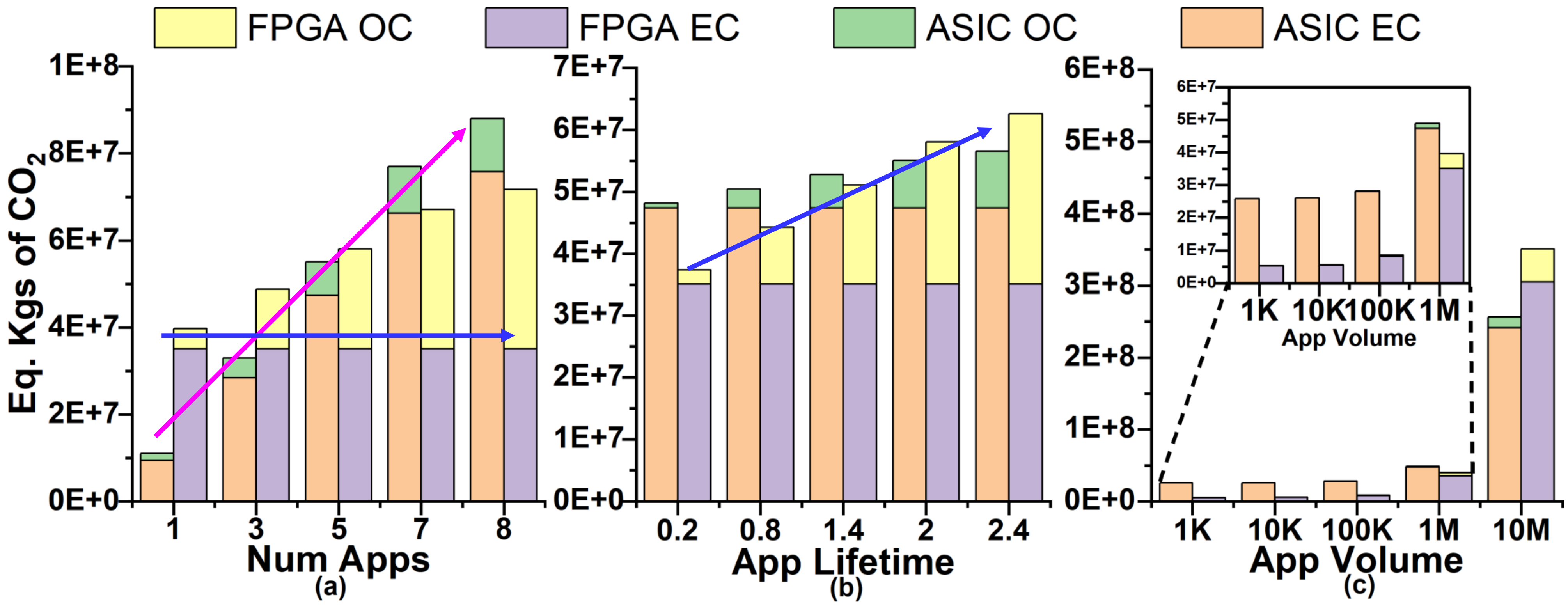


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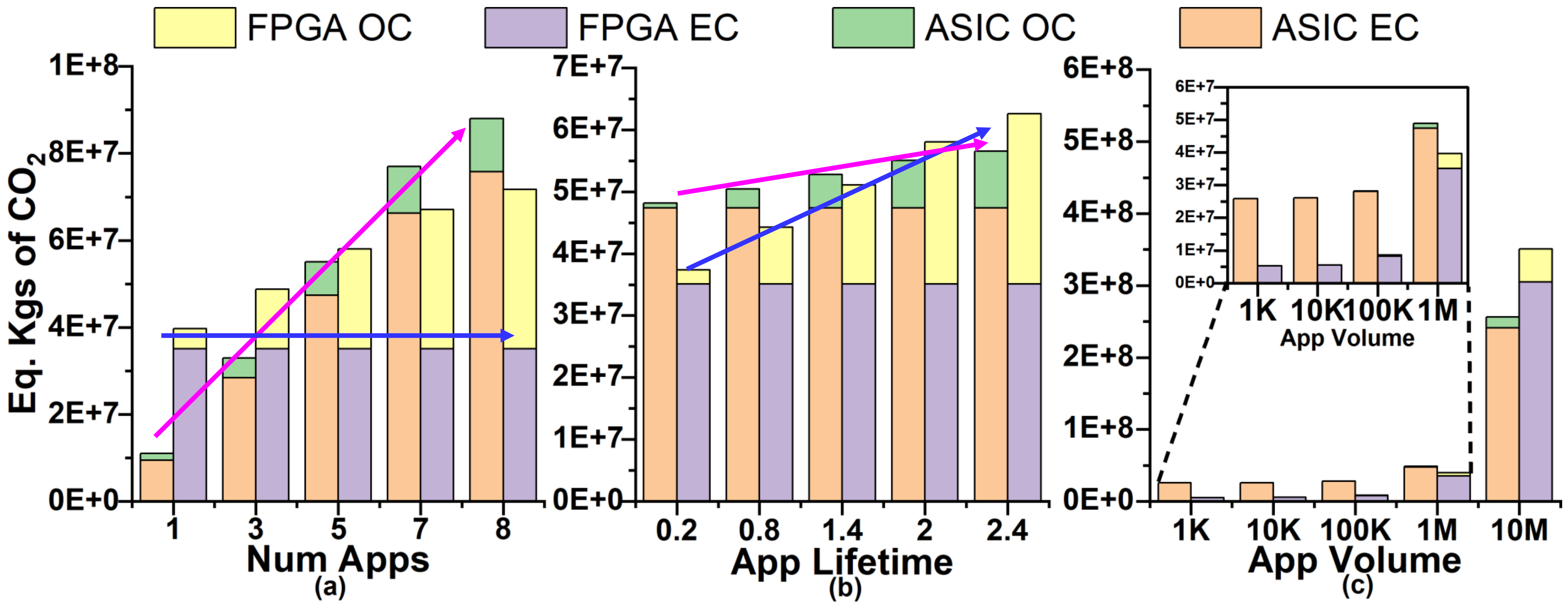


- Embodied CFP of FPGA stays the same, while that of ASIC increases as the number of applications increase
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# Conclusion and key takeaways

- Embodied CFP of the FPGA is amortized across multiple applications unlike ASICs
- FPGAs are a good solution sustainably compared to ASICs if we have 6 or more applications for DNN test case
- Considering DNN if the probability of changing applications frequently is less than 1.6yrs, FPGAs are good sustainable solutions
- FPGAs are environmentally sustainable for lower application volume

https://github.com/ASU-VDA-Lab/GreenFPGA

**Scan QR code for GreenFPGA**